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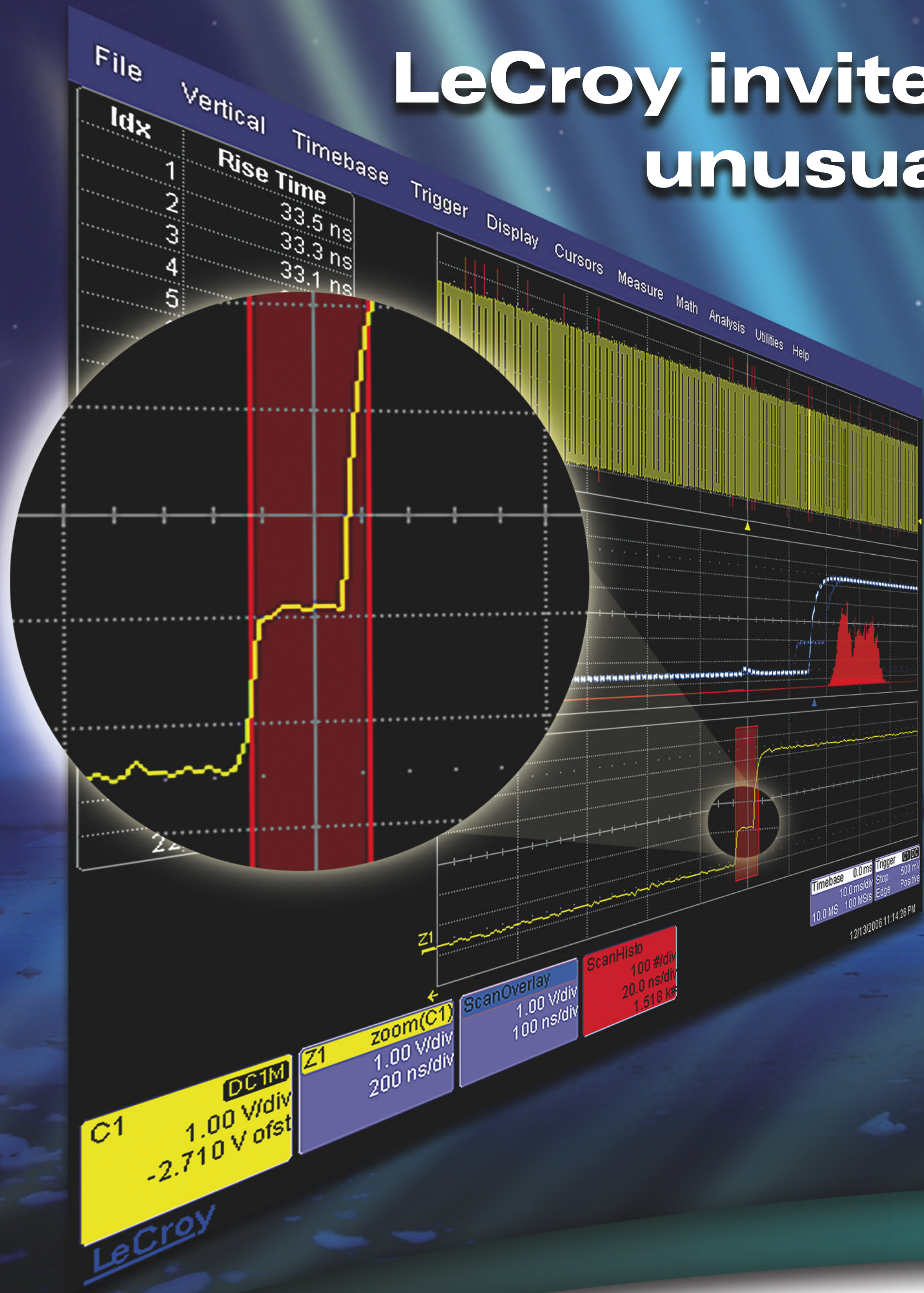

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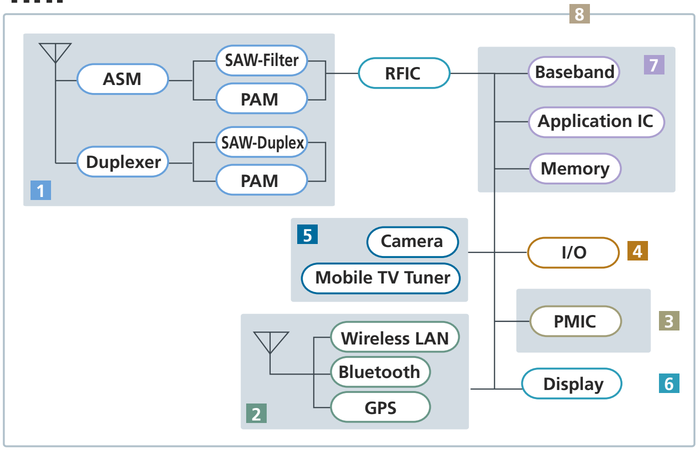

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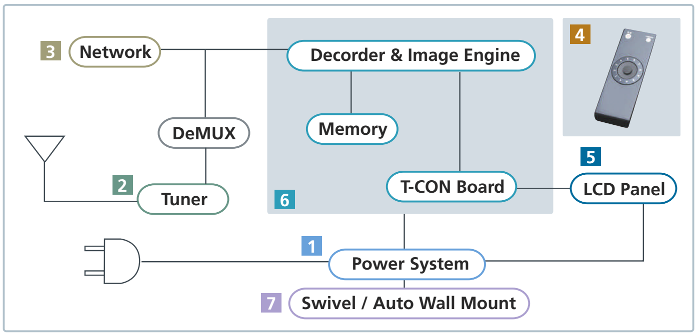

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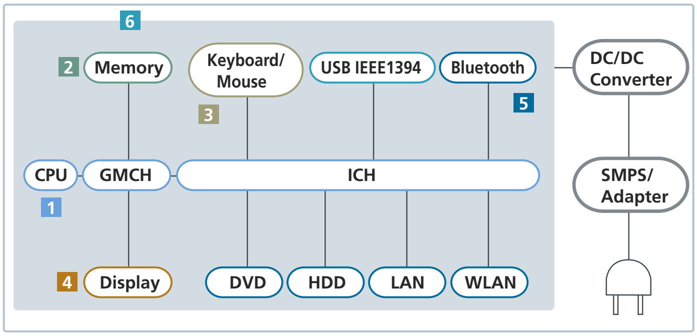

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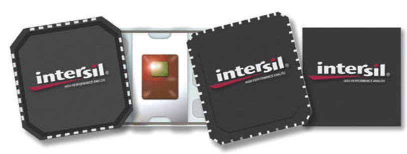

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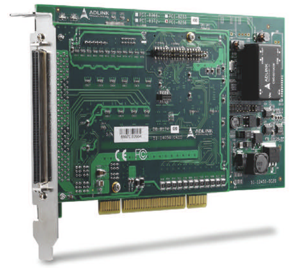

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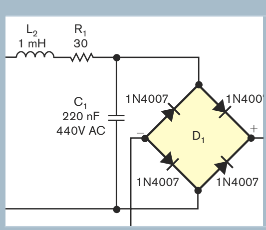

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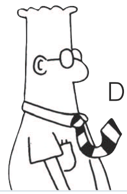

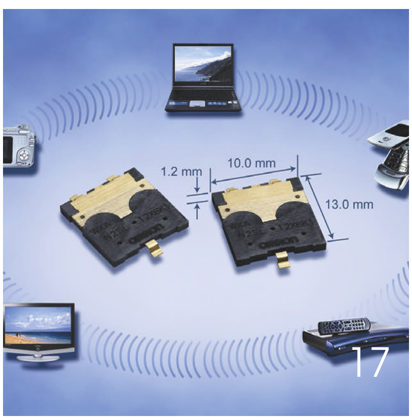

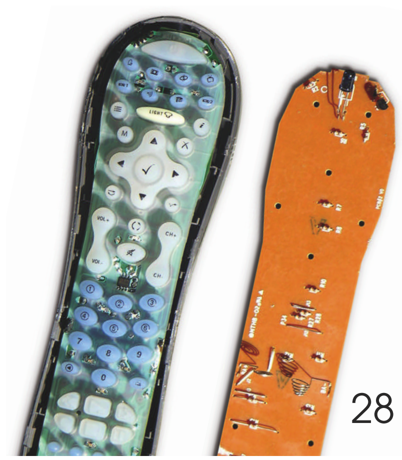

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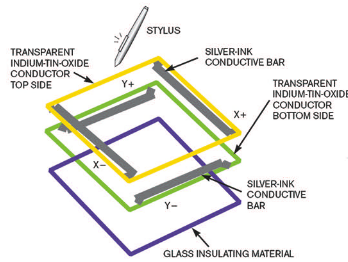

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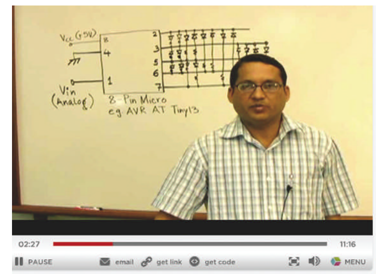

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BY MAURY WRIGHT, EDITORIAL DIRECTOR

H1-B questions hit *EDN* readers' hot button

A couple of times this year, I've highlighted research that *EDN* has conducted on the market or on engineers. We have more such material coming your way with a global engineering-salary-and-career survey that we will present next month. In the meantime, we conducted a one-day career-oriented survey on our Web site on Sept 26, and this column presents a few results from that survey. In particular, the subject of H1-B visas drew a number of interesting responses.

I thought that we had carefully considered what we would ask about H1-B visas, though your response indicated that we had failed. We settled on two questions. First, we asked, "Do you believe the government should expand the number of H1-B visas?" Second, we asked respondents to choose among three responses that best summed up their feelings and experiences with H1-B visas. The choices were: "I am working on an H1-B visa, and it has been a fantastic opportunity"; "I believe that we are short on qualified engineers in the United States, and I support the idea of increasing the number of H1-B visas"; and "My career was harmed when I lost an opportunity to another engineer that was a part of the H1-B program."

First, I want to assure you that we had no ulterior motive with this survey. One reader suggested, "[The second question] is very biased. I believe that we are short on engineers, but expanding the H1-B is not the answer; convincing kids to enter engineering is. You guys must already have written the result and are waiting for the survey to support it." In fact, *EDN* as a whole has no position on H1-B visas. As several of you suggested, we should have offered the option on the first question to answer in a way other than "yes" or "no." And we offered too few choices in the second question.

For better or for worse, here are the results we gathered. To the yes/no question, 48.9% of you answered that, yes, the government should expand the H1-B offerings, and 51.9% answered no. In response to the second question, the answers came in at 3.5% for those working on an H1-B visa and believing it to be a great opportunity, 58.3% for those who believe that we should increase the number of H1-B visas because the United States is lacking in qualified engineers, and 38.2% who believe their career suffered because of the H1-B program. Keep in mind, though, that many of you couldn't match your feelings to the answers we offered.

A number of readers indicated that they believe that the United States has an acute shortage of engineers, whereas they call into question the ideals behind and the execution of the H1-B program. One respondent noted, "The H1-B program has many holes. It is like indentured servitude. Many of my colleagues in the past who were H1-B holders were underpaid compared to others in similar positions. They were forced to work long hours and weekends as they were threatened with losing their jobs. If they lost their job, they lost their place in the permanent-residency line." Another added, "H1-B can be a good resource; however, it appears to be abused by hiring non-US workers at a lower wage in some situations."

A number of respondents pointed out that we should solve an engineering shortage by encouraging more students to enter the engineering field and by using available talent. One noted, "I believe there is a shortage of qualified engineers, but most companies are not willing to hire laid-off workers. I think there is an unfair bias against these workers. From my wife's experience, the potential employers that do give an interview are actually stealing ideas from these experienced workers and then not giving them a chance."

On a positive note, most respondents like their job and want to encourage young engineers. One noted, "I believe there is strong need for informing young students, high-school age to early college, of all the different types of engineering jobs that are available. … Engineering is about solving problems, and we need to educate people on how fun that can be!"

To view the results of our survey, go to www.edn.com/071025ed2. EDN

Contact me at mgwright@edn.com.

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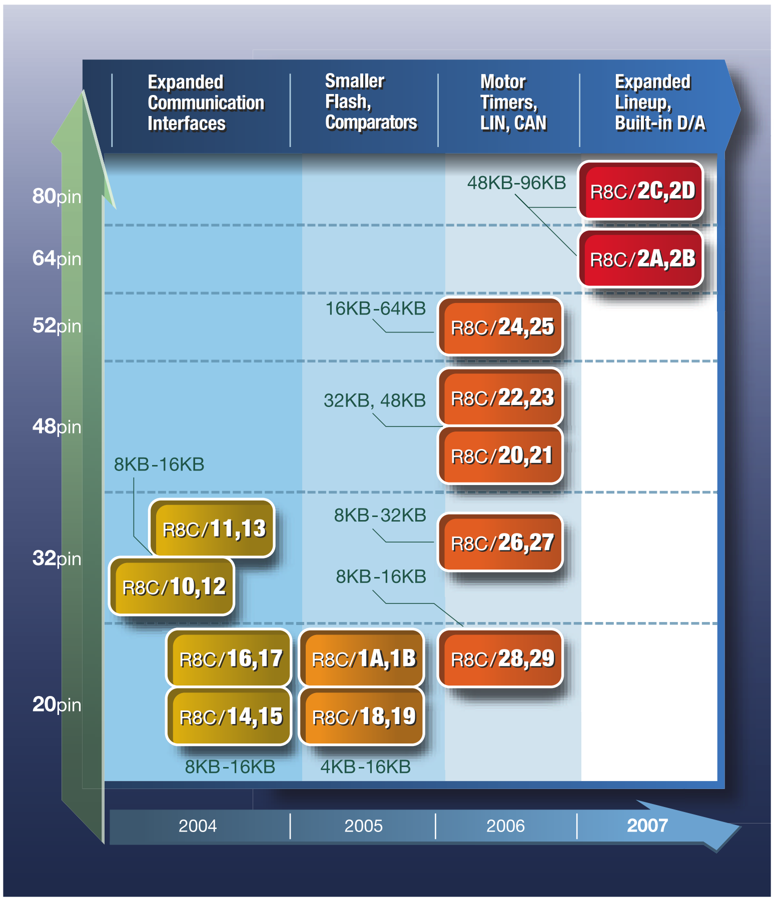

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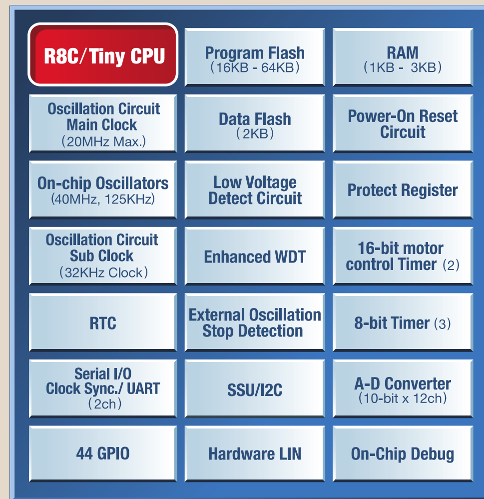

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Design Challenges of Switching LED Drivers [Part 1 of 2]

Application Note AN-1656

Chris Richardson, Applications Engineer

Using a switching regulator as an LED driver requires the designer to convert a voltage regulator into a current regulator. Beyond the challenge of changing the feedback system to control current, the LEDs themselves present a load characteristic that is much different than the digital devices and other loads that require constant voltage. The LED WEBENCH® online design environment predicts and simulates the response of an LED to constant current while taking into account several potential design parameters that are new to designers of traditional switching regulators.

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In the first step of the LED WEBENCH tool, "Choose Your LEDs", an LED is selected with a standard forward current, I_F. This default value is provided by the LED manufacturers, and in most cases it represents the testing condition for that LED. Typical values for high-power LEDs are 350 mA, 700 mA, and 1000 mA.

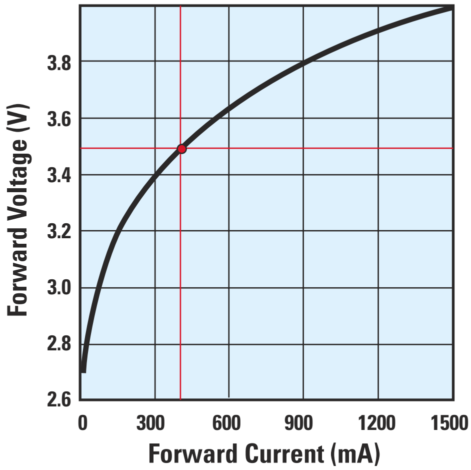

Figure 1. V-I Curve with Typical V_F and I_F

Not all designs will use a standard current, however. The designer can select a different LED current, and then the forward voltage will change in the V_{LED} box under step 2. The change in voltage comes from LEDs' V-I curve. *Figure 1* shows a curve from a 5W white (InGaN) LED that differs from the curves normally found in LED datasheets. LED manufacturers provide these curves, but they are often shown as I-V curves with voltage as the independent quantity. In *Figure 1*, forward current is the independent variable, reflecting the fact that in LED drivers current is controlled, and voltage is allowed to vary. The cross-hairs intersect at the standard/typical I_F and V_F values of 350 mA and 3.5V, respectively.

Once the V_F of the LEDs has been determined from the V-I curve, the LED driver's output voltage is calculated using the following formula:

$$V_O = n \times V_F + V_{SNS}$$

In this equation, 'n' is the number of LEDs connected in series, and 'V_{SNS}' is the voltage drop across the current sense resistor.

Designing for $V_{O\text{-}MIN}$ and $V_{O\text{-}MAX}$

In practice, the typical value of V_F changes with forward current. Further analysis of total output voltage is needed because V_F also changes with process and with the LED die temperature. The more LEDs in series, the larger the potential difference between $V_{O\text{-}MIN}$, $V_{O\text{-}TYP}$ and $V_{O\text{-}MAX}$. An LED driver must therefore be able to vary output voltage over a wide range to maintain a constant current. I_F is the controlled parameter, but minimum and maximum output voltage must be predicted in order to select the proper regulator topology, IC, and passive components.

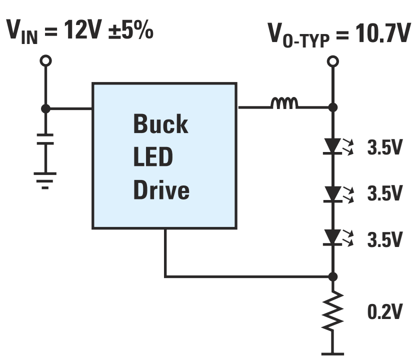

Figure 2. $V_{IN\text{-}MIN} > V_{O\text{-}TYP}$, Buck Regulator Works

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A typical example that can lead to trouble is driving three white (InGaN) LEDs from an input voltage of 12V ±5%. In ***Figure 2,*** each LED operates at the typical V_F of 3.5V, and the current sense adds 0.2V for a V_O of 10.7V. Minimum input voltage is 95% of 12V, or 11.4V, meaning that a buck regulator capable of high duty cycle could be used to drive the LEDs.

However, a buck regulator designed for the typical V_O will be unable to control I_F if $V_{O\text{-}MAX}$ exceeds the minimum input voltage. The same white LEDs with a typical V_F of 3.5V have a $V_{F\text{-}MAX}$ of 4.0V. Headroom is tight under typical conditions, and the buck regulator will lose regulation with only a small increase in V_F from one or more of the LEDs ***(Figure 3)***.

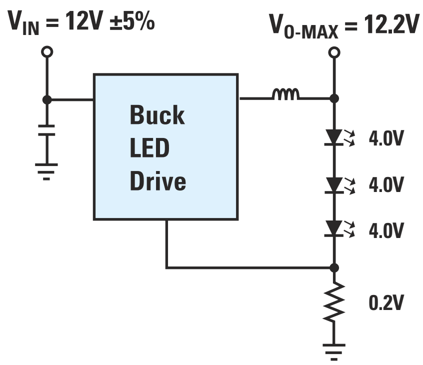

Figure 3. $V_{IN\text{-}MIN} < V_{O\text{-}MAX}$, Buck Regulator Fails to Regulate

Pitfalls of Parallel LED Arrays

Whenever LEDs are placed in parallel, the potential exists for a mismatch in the current that flows through the different branches. The forward voltage, V_F, of each LED varies with process, so unless each LED is binned or selected to match V_F, the LED or LED string with the lowest total forward voltage will draw the most current ***(Figure 4)***. This problem is compounded by the negative temperature coefficient of LEDs (and all PN junction diodes). The LEDs that draw the most current suffer the greatest increase in die temperature. As their die temperature increases, their V_F decreases, creating a positive feedback loop. Elevated die temperature both reduces the light output and decreases the lifetime of the LEDs.

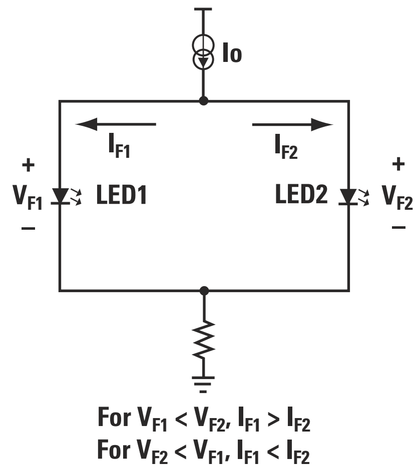

Figure 4. Mismatched LEDs in Parallel

The system in ***Figure 4*** also illustrates a potential over-current condition if one of the LEDs fails as an open circuit. Without some protection scheme, the entire drive current I_O will flow through the remaining LED(s), likely causing thermal overstress. Likewise, if one of the LEDs fails as a short circuit, the total forward voltage of that string will drop significantly, causing higher current to flow through the affected branch.

To maintain safety and reliability in a parallel LED system, forward voltage should be binned or matched. Fault monitoring should detect LEDs that fail as either short or open circuits. Finally, the entire array should have evenly distributed heat sinking, to ensure that V_F change with respect to die temperature occurs uniformly over all the LEDs. ■

To read part 2 of this application note, visit www.national.com/ae4

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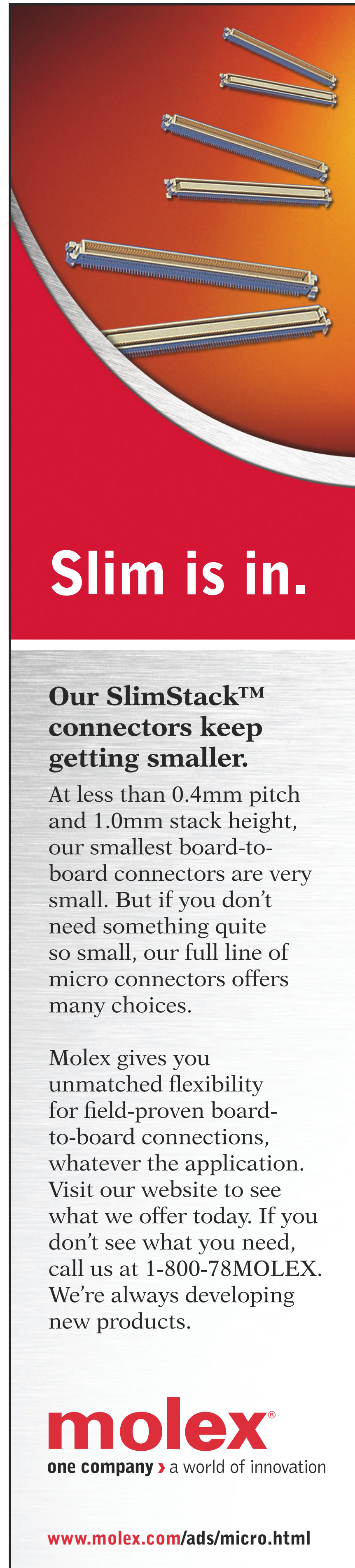
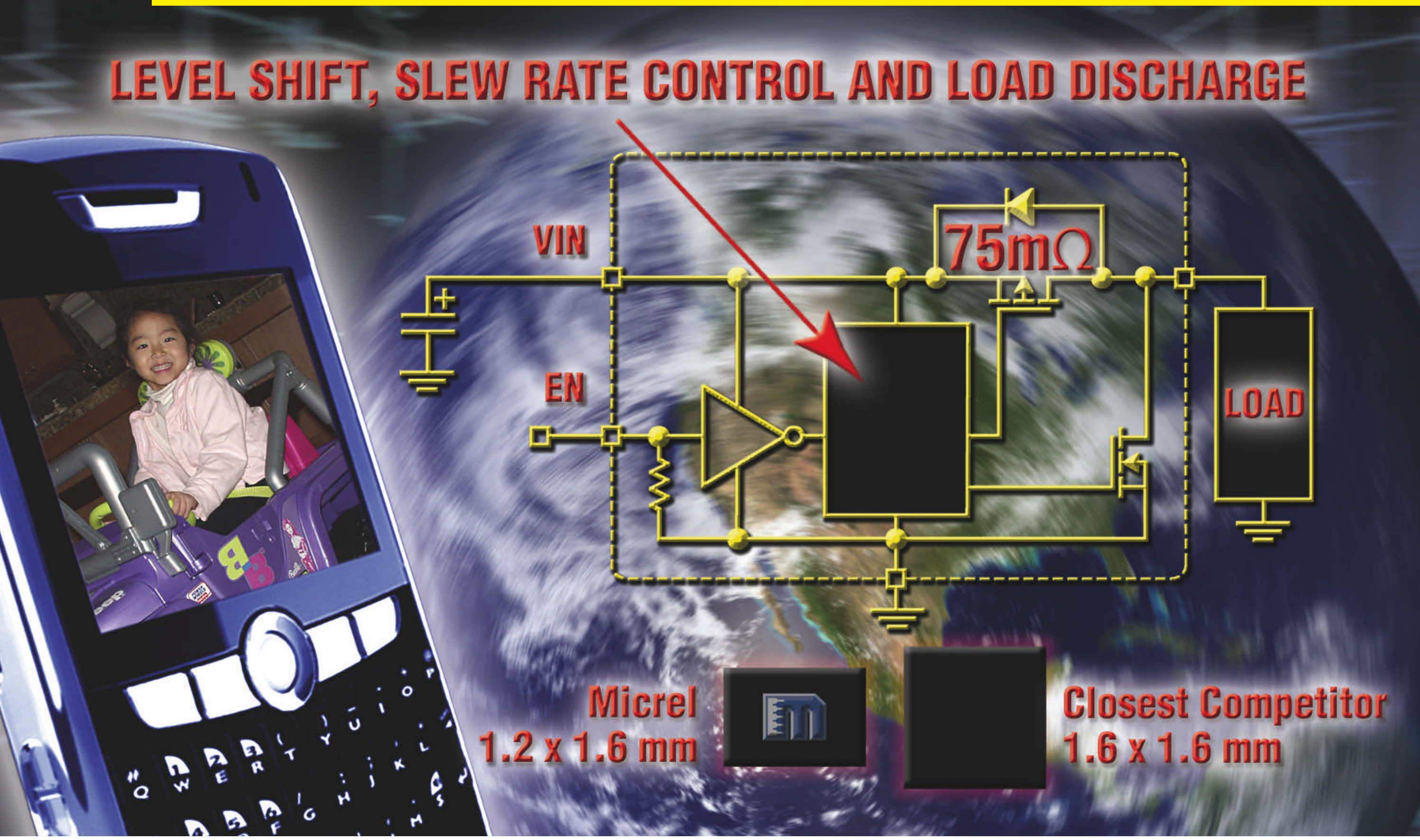


Get On The High Side With Micrel

High-side load switches offer the lowest $R_{DS(ON)}$, high efficiency and smallest package



Battery-powered portable devices rely upon high-side load switches to manage the power path. These high-side load switches are required to have high efficiency and small footprint in order for the portable devices to extend battery running time and save space.

Micrel Semiconductor offers a full portfolio of P-channel FET high-side load switches targeting the battery-powered portable device market. The latest addition, the MIC94060/1/2/3 product family, is industry-leading in all the key parameters that are of interest to designers.

The MIC94060/1/2/3 P-channel high-side load switch family has established itself as the performance leader in the world of battery-powered portable devices, including feature-rich mobile handsets, mobile GPS equipment, and consumer entertainment gadgets.

The Good Stuff:

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- Smallest Package
- Lowest Shutdown Current
- Slew Rate Control at Startup
- Active Load Discharge at Shutdown

For more information, contact your local Micrel sales representative or visit Micrel at: www.micrel.com/ad/mic9406x.
Literature 1 (408) 435-2452 Information 1 (408) 944-0800

	MIC94060	MIC94061	MIC94062	MIC94063
V_{IN}	1.7V to 5.5V	1.7V to 5.5V	1.7V to 5.5V	1.7V to 5.5V
$R_{DS(ON)}$ - SC70	75mΩ	75mΩ	75mΩ	75mΩ
$R_{DS(ON)}$ - MLF	85mΩ	85mΩ	85mΩ	85mΩ
I_{MAX}	2A	2A	2A	2A
$I_{SHUT-SUPPLY}$	2nA	2nA	2nA	2nA
$I_{SHUT-LEAKAGE}$	2nA	2nA	2nA	2nA
t_{ON-DLY}	0.85µs	0.85µs	700µs	700µs
$t_{ON-RISE}$	1µs	1µs	800µs	800µs
$t_{OFF-DLY}$	100ns	100ns	60ns	60ns
$t_{OFF-FALL}$	60ns	60ns	60ns	60ns
Package	1.2x1.6 MLF®-4 SC-70-6	1.2x1.6 MLF®-4 SC-70-6	1.2x1.6 MLF®-4 SC-70-6	1.2x1.6 MLF®-4 SC-70-6
FEATURES				
Slew Rate Control			✓	✓
Fast Turn On	✓	✓		
Load Discharge		✓		✓

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EDITED BY FRAN GRANVILLE

pulse

INNOVATIONS & INNOVATORS

Small antennas suit FM, UWB bands

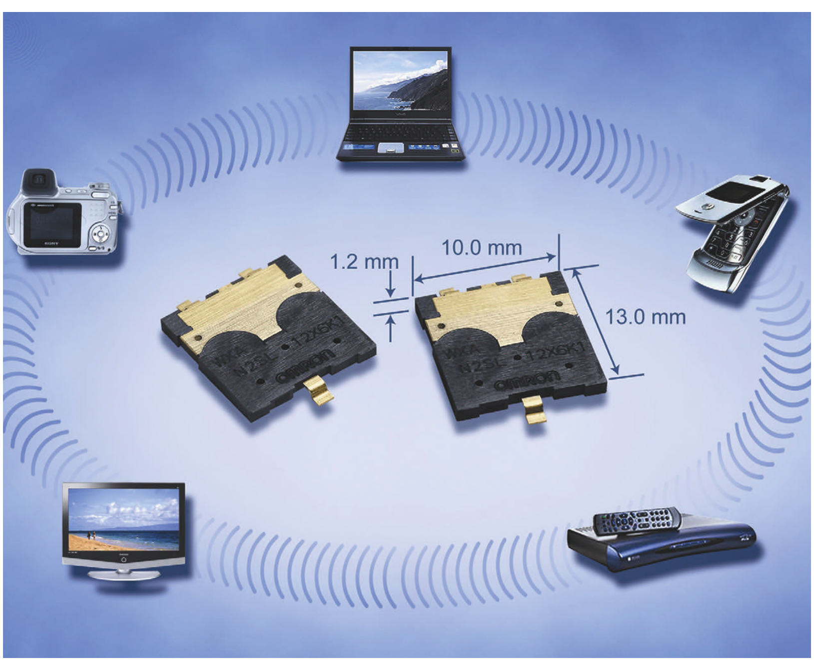
Antennas continue to get smaller and cheaper. For example, Laird Technologies' miniature Activv internal antenna circuit combines FM, impedance matching, and signal amplification. It replaces the company's RadioAnt antenna and provides 5-dB greater sensitivity over a frequency range of 76 to 108 MHz in a 25% smaller package. Prices range from 50 cents to $2 (volume quantities), depending on the level of customization.

Omron's surface-mounted polymeric antenna, the WXA-N2SL, transmits and receives in the 3.1- to 4.9-GHz UWB (ultrawideband) WiMedia Alliance (www.wimedia.org) BandGroup 1. The antenna's filter-assistance function suppresses out-of-band noise by 50% or more, enabling high-quality communications between these wireless devices even in noisy environments. The antenna measures 10×13×1.2 mm with a VSWR (voltage-standing-wave ratio) of less than 2.5 in the 3.1- to 4.9-GHz band and greater than 6 in the 7- to 11-GHz band. The linearly polarized device has a feed impedance of 50Ω and sells for approximately $3 (100).

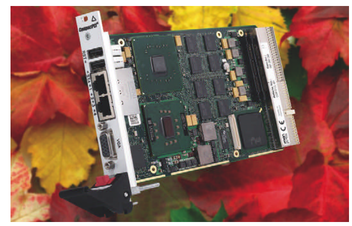
—by Margery Conner

▷**Laird Technologies**, www.lairdtech.com.

▷**Omron**, www.components.omron.com.



Omron's WXA-N2SL UWB antenna suits applications such as wireless-USB dongles, hubs, PCs, mobile equipment, and digital-home appliances.



The latest F18 CompactPCI Express single-board computer incorporates Intel's CoreT2 Duo processor and features accelerated graphics performance.

CompactPCI Express module boasts dual processors

Competing for industrial applications such as monitoring, visualization, control, and test and measurement, MEN Micro recently introduced the F18 CompactPCIe (PCI Express) single-board computer. The 64-bit board employs Intel's 2.2-GHz T7500 CoreT2 Duo processor and includes a 667/800-MHz front-side bus and the mobile Intel 965GM Express chip set with a built-in graphics-media accelerator. The 32-bit, 33-MHz F18 system-slot or stand-alone board needs only one slot on the CompactPCIe bus. Designers can combine the F18 with a PCIe mezzanine card for use as a system-slot board in CompactPCIe systems.

Front-panel I/O includes VGA graphics, two GbE (Gigabit Ethernet) ports that connect through PCIe, and two USB 2.0 interfaces. Additional I/O is available on mezzanine cards and includes DVI (digital-video interface), audio, additional USB interfaces, UART interfaces, and FireWire. The F18 enters the market with board-support packages for Windows, Linux, and VxWorks. Prices start at $3719 (one) for systems with 4 Gbytes of system memory.

—by Warren Webb

▷**MEN Micro Inc**, www.menmicro.com.

Software opens your eyes to serial-data-link-error sources

Tektronix has announced a new end-to-end high-speed serial-data-analysis-software package with test capabilities that extend from transmitter to receiver, including the connecting channel. The package, 80SJNB Advanced, is the latest version of 80SJNB (8000-series instrument software for jitter, noise, and BER, or bit-error-ratio) measurement. It runs on the manufacturer's DSA8200 digital serial analyzer, an ultrawide-bandwidth sequential-sampling oscilloscope. Combined with the DSA8200's TDR/TDT (time-domain reflectometry/time-domain-transmission) and S (scattering)-parameter support through iConnect software, 80SJNB Advanced provides engineers with what Tektronix calls the first complete SDLA (serial-data-link-analysis) package to ensure that a readable signal reaches the receiver.

The package incorporates FFE (feedforward equalization) and DFE (decision-feedback equalization) to provide a virtual view of the signal as it appears at the comparator inside the receiver. Emulation of the interconnect channel makes it possible to measure how the transmitter performs with different interconnects. Support for fixture de-embedding enables virtual probing of inaccessible points. The complete SDLA offering provides the fundamental measurements to validate equipment compliance with high-speed-serial standards, such as 10-GbE (Gigabit Ethernet), PCI Express, and SATA (serial advanced-technology attachment), enabling the development of higher performance digital products.

"Because of [emerging] serial-interface standards' higher speed, test fixturing and small differences in the channel can cause significant variations in signal characteristics," says Eric Kvamme, principal engineer at LSI Corp (www.lsi.com). "With the ability to de-embed fixtures, emulate channels, and model equalization on the high-speed scope, Tektronix's new SDLA tools, including the DSA8200 with 80SJNB Advanced software, help us to more quickly characterize our serial products and evaluate their performance under additional scenarios and thus provide our customers with more robust [ways to meet their communications requirements]."

"Equalization" is a broad term that describes several techniques for manipulating the signal shape to overcome the channel's frequency-dependent loss. At the receiver, this loss changes the NRZ (non-return-to-zero) data signal's shape from the desired square wave to a severely distorted, closed-eye waveform. The 80SJNB Advanced package provides FFE and DFE on the receiver side and supports generation and measurement of pre- and de-emphasis on the transmitter side.

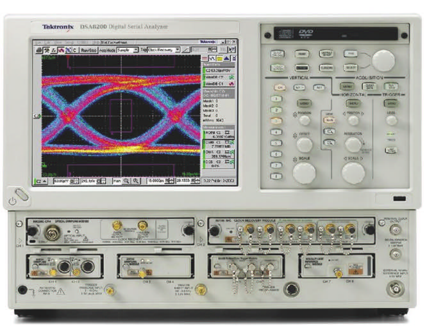
Another capability of the software is channel emulation, which gives users a pushbutton way to see waveform impairments caused by channel (interconnect) transmission loss. Through channel emulation, engineers can acquire a signal at the transmitter output and distort it by sending it through an emulated channel, which can be a backplane, a connector, or anything that TDR/TDT or S-parameters can describe. This approach allows verifying of link performance at the channel end without waiting for hardware to become available. Final analysis employs BER eye diagrams and the jitter- and noise-decomposition capabilities of 80SJNB Advanced.

Acquisition and advanced analysis of complex signals are increasingly necessary on transmitters with SSC (spread-spectrum clocking), which is common in desktop and laptop PCs, and in the SATA and PCI Express standards. The DSA8200 with 80SJNB Advanced provides engineers with a sampling scope that can perform SSC acquisitions and jitter analysis.

The US suggested price for the 80SJNB Advanced package is $15,800 when you order it with a new DSA8200. Current 80SJNB software licensees can download a free version of 80SJNB Essentials from www.tek.com or can upgrade to 80SJNB Advanced for $4900. The package supports older Tektronix sampling mainframes, though some may require upgrades.

—by Dan Strassberg

▷**Tektronix Inc**, www.tek.com.



With the 80SJNB Advanced and iConnect software packages, the DSA8200 digital serial analyzer becomes what the manufacturer calls the first complete serial-data-link-analysis package to ensure that a readable signal reaches the receiver.

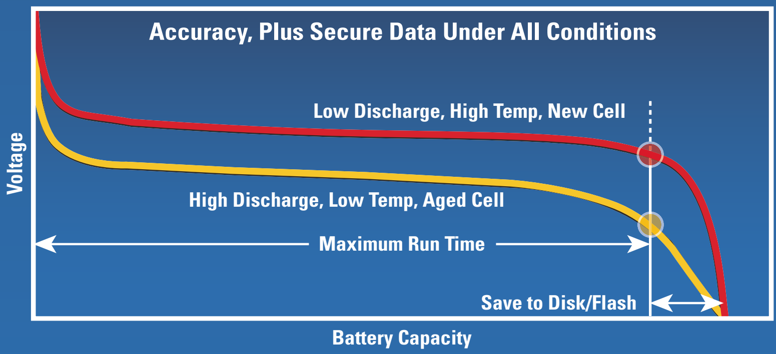
DILBERT By Scott Adams

Run Smarter, Run Longer

System-Side Impedance Track™ Battery Fuel Gauge

HIGH-PERFORMANCE ANALOG >> YOUR WAY™ (PRODUCTS · APPLICATIONS · SUPPORT)

The new **bq27500** system-side battery fuel gauge from Texas Instruments accurately predicts battery run time in smart phones and other handheld electronic devices. Featuring TI's patented Impedance Track technology, the IC maintains accuracy for the entire life of the battery under all conditions, reserves energy to save data and never sacrifices run time.



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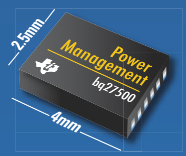

For samples and evaluation modules, visit >>
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Synopsys releases SystemC-model library

Synopsys is broadening its DesignWare silicon and verification-IP (intellectual-property) portfolio with the DesignWare system-level library, a group of SystemC transaction-level models. This introduction signals a change in the company's attitude: Synopsys once backed SystemC's main rival, SystemVerilog, and acquired that software's inventor, CoDesign. In the 1990s, when CoWare (www.coware.com) introduced SystemC, Synopsys embraced it, co-founded the OSCI (Open SystemC Initiative, www.systemc.org), and contributed an open-source simulator to the organization. Markus Willems, product-marketing manager for system-level solutions at Synopsys, acknowledges that the company shifted its focus toward SystemVerilog and away from SystemC as a next-generation language. He emphasizes that Synopsys did not abandon SystemC, however. The company has for many years supported the language in its simulation lineup. "With the upswing of the transaction-level-modeling concept … the market's become highly interesting to Synopsys," he says. "Now, the concept of building virtual platforms for prehardware-software development is coming to maturity, and the market is requesting a SystemC-based solution."

Attesting to the focus on SystemC, Synopsys two years ago acquired Virtio Corp and its Virtual Platform technology, which allows design groups to create a transaction-level virtual prototype of a device. The groups then send one copy of the prototype to hardware designers to begin the hardware design and another to software groups to develop firmware, an operating system, drivers, and applications for the platform. The technology's most notable success has been with Texas Instruments (www.ti.com), which uses the tool to create architecture derivatives of its OMAP (Open Multimedia Applications Platform). Originally, Virtio developed a proprietary transaction-level model for customer platforms but supported SystemC. However, customers

> "The technology's most notable success has been with Texas Instruments.

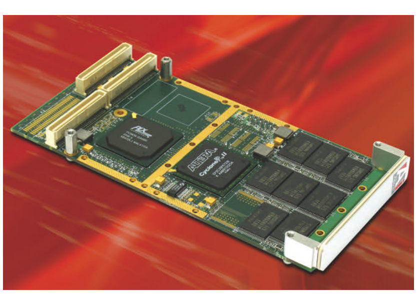
are now opting for SystemC over other types of transaction-level models. With DesignWare, Synopsys hopes to help Virtio customers more quickly build platforms and help companies using SystemC models to develop their own architectures, because the models work with any IEEE 1666 SystemC-compliant simulators.

The library comprises SystemC transaction models of commonly used IP blocks and functions. It includes ARM7-TDMI, ARM920T, ARM926EJ-S, ARM946E-S, ARM-1136-JFS, and ARM1176JZFS processor models; ARM AMBA (Advanced Microcontroller Bus Architecture), AHB (advanced high-performance bus), and AMBA APB (advanced peripheral bus); peripherals; a UART interface; an interrupt controller; and an I²C interface. Synopsys has also added several models of its DesignWare cores, including models for USB 2.0, High Speed OTG (On-The-Go), SATA (serial advanced-technology attachment), and AHCI (advanced host-controller interface). The library also includes platforms combining these functions with others. Preassembled platforms include the VPMP (virtual-platform-multimedia-player) demo, the VPAI (virtual platform for ARM integrator), the VPQSML (virtual-platform quick-start multilayer), and the VPTest (virtual-platform test).

Traditionally, Synopsys has drawn revenue from creating these models for customers such as TI. The new library functions will allow customers to fill most of their platforms with models from the library, but Willems believes that customers will still likely hire Synopsys services to model unique logic functions in their designs or functions that the library lacks.
—by Michael Santarini

▷**Synopsys**, www.synopsys.com.

Mezzanine card boosts memory performance



The high-density, low-power M222 flash-memory PCI mezzanine card provides data-transfer rates of more than 130 Mbytes/sec through FPGA-based DMA controllers.

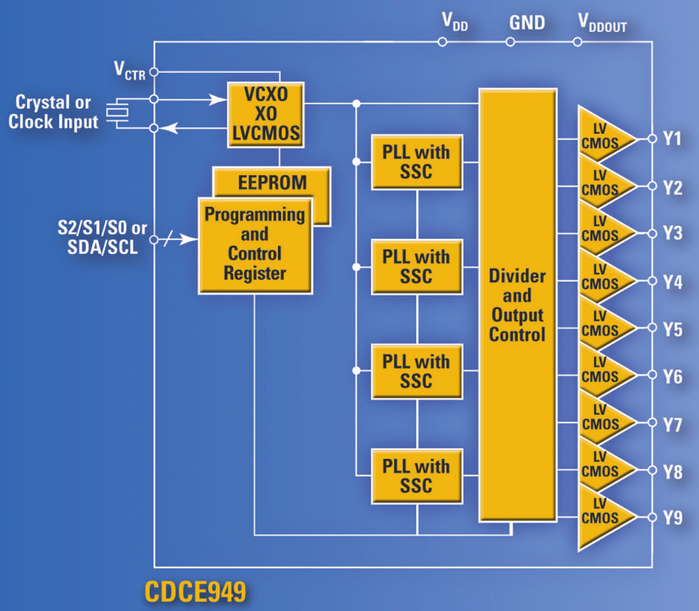
Targeting use in high-density-local-storage applications, such as tactical area maps, radar images, and software-programmable radio-electronic-intelligence data, Aitech Defense Systems' new M222 PMC (PCI mezzanine card) provides sustained data transfers as fast as 130 Mbytes/sec and consumes less than 7W. The board incorporates as much as 64 Gbytes of NAND-flash memory in two independent banks with integrated FPGA-based DMA (direct-memory-access) controllers. The M222 provides full file-system read/write emulation, automatic block management, and interleaved DMA of as many as 32 memory banks.

An automatic wear-leveling flash-driver package ensures the uniform balancing of write/erase cycles across the entire device to eliminate excessive wear from repeated write/erase cycles to any individual block. The onboard DMA controller provides "write-ahead" buffers for write/erase operations to increase data throughput. An optional memory-manager software package automatically treats the flash memory as the system's disk drive to provide real-time-operating-system support. The single-slot PMC module connects to, and takes all of its power from, the CompactPCI, VMEbus, or PCI baseboard. The price for an 8-Gbyte M222 starts at $5670. Delivery is from stock to four weeks.**—by Warren Webb**

▷**Aitech Defense Systems Inc**, www.rugged.com.

Flexible Clock Generators

Multiple I/O-V and Programmability Ease System Design



Applications

– Digital media systems (audio/video)
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– Streaming media (DVD-P/R)
– GPS receivers
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– TI DSP, OMAP™ and DaVinci™ media processors

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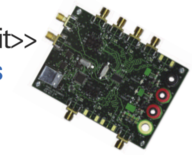
– Spread Spectrum Clocking (SSC) reduces affects of EMI
– I²C and EEPROM programmability
– On-chip Voltage Controlled Crystal Oscillator (VCXO)
– 14-, 16-, 20- and 24-pin TSSOP

HIGH-PERFORMANCE ANALOG >> YOUR WAY™ (APPLICATIONS, SUPPORT, PRODUCTS)

Texas Instruments produces a portfolio of low-power, low-jitter, programmable clock generators capable of generating up to nine output clocks from a single input frequency – each output is programmable in-system for any clock frequency up to 230MHz. This level of functionality provides the system designer with capabilities previously unavailable in clock/timing products.

Device	Supply Voltage (V)	I/O Voltage (V)	# of PLL	# of Outputs	Output Frequency (MHz)	Temperature Range (°C)	Package (TSSOP)
CDCE949	1.8	2.5/3.3	4	9	230	–40 to +85	24
CDCE937	1.8	2.5/3.3	3	7	230	–40 to +85	20
CDCE925	1.8	2.5/3.3	2	5	230	–40 to +85	16
CDCE913	1.8	2.5/3.3	1	3	230	–40 to +85	14
CDCEL949	1.8	1.8	4	9	230	–40 to +85	24
CDCEL937	1.8	1.8	3	7	230	–40 to +85	20
CDCEL925	1.8	1.8	2	5	230	–40 to +85	16
CDCEL913	1.8	1.8	1	3	230	–40 to +85	14

For samples, evaluation modules, visit>>
www.ti.com/programmableclocks
800.477.8924, ext. 13971



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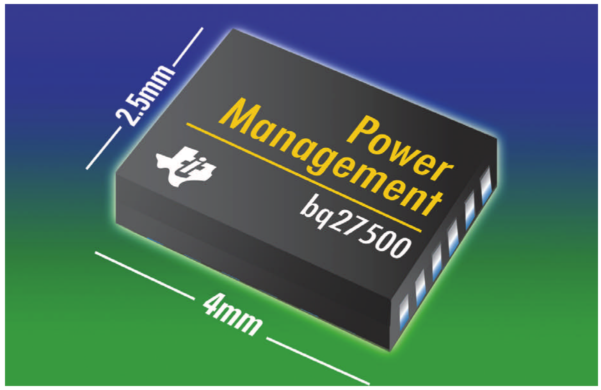
Battery-fuel-gauge chip provides 99% accuracy

Battery-gauge ICs for lithium-ion-battery packs have always involved complex algorithms. For example, battery gauges in laptop computers and cell phones measure current, voltage, and temperature and integrate the current over time to find the charge. They must model the cell's reaction to discharge rate, temperature, age, and self-discharge rate, and they must relearn the full-charge capacity over time. They also must predict and accumulate the error for all of these numbers.



The bq27500 system-side battery-fuel gauge from Texas Instruments uses the company's Impedance Track technology to accurately predict battery life.

Texas Instruments addresses this complexity and bets that user demand for more accurate gauging will make consumer-electronic vendors eager to incorporate its new gauges, which employ the company's Impedance Track technology. The new system-side bq27500 incorporates Impedance Track to directly measure the effects of discharge rate, age, and temperature on battery charge. This sophisticated direct-measurement technique allows the gauge to calculate the effect on remaining and full-charge capacity with no modeling or learning. TI claims that the technology provides 99% accuracy in gauging remaining battery charge, and that figure is accurate, according to Robin Tichy, PhD, technical-marketing manager at battery-pack-design house Micro Power (www.micro-power.com).

Tichy points to applications in medical electronics for life support as appropriate uses for Impedance Track. These applications require batteries that provide a precise countdown to 30 minutes before the battery power runs out. As a result, most life-support electronics rely on sealed lead-acid backup batteries rather than on lithium-ion devices because lead-acid batteries' predictably constant slope makes them easy to gauge. In contrast, lithium-ion batteries' discharge profile is constant until just before the batteries completely discharge, when it decreases sharply. However, TI's Impedance Track provides an accurate measurement on the remaining battery power, allowing the use of Micro Power's lithium-ion-backup-battery packs in critical medical applications, according to Tichy.

—by Margery Conner

▷**Texas Instruments**, www.ti.com.

AC/DC converters efficiently handle load changes with digital-control loop

Power-conversion efficiency is important in server farms in which more than 10,000 blade servers share the same facility: For every watt at the load, the farm consumes 2W of energy due to delivery losses, and an increase in power-conversion efficiency results in double the overall energy savings. To address these problems, Coldwatt based its new 1U ac/dc-converter, 750 and 1625W power subsystems on a digital-power-conversion platform. A Silicon Labs (www.silabs.com) C8051F30x microcontroller powers the platform, and Coldwatt officials claim that the power system is more efficient than traditional analog-loop power converters.

Coldwatt's 1625W power module delivers 90% efficiency at 20% or higher loads, an important feature for redundant supplies, which seldom operate at full load.

A power converter with a digital-control loop has no clear advantage over traditional analog closed-loop systems powering a fixed load, because you can tune the analog loop and filter to match the load. However, when the load can swing widely, a power converter with a digital loop can be more efficient over the load swings. For example, in a redundant supply for a server farm, the redundant supply seldom operates at full load; its load instead typically varies from 10 to 40% of full load. In contrast, Coldwatt's 1625W power module delivers 90% efficiency at 20% or higher load, which the company claims is a 20% efficiency advantage in this range over analog supplies. Further, the Coldwatt supplies can quickly react to a condition that requires the redundant supply to switch to a full load. The supplies' efficiency and active power-factor correction qualify them for the 2009 Climate Savers (www.climatesaverscomputing.org) industry initiative for data-center supplies.

In addition, the supplies' black box continuously monitors and records critical power parameters, such as input voltage, output voltage, and temperature for increased traceability and fault analysis. The 1625W, 1U ac/dc-power subsystem sells for $317, and the 750W, 1U supply sells for $157 (1000).

—by Margery Conner

▷**Coldwatt**, www.coldwatt.com.

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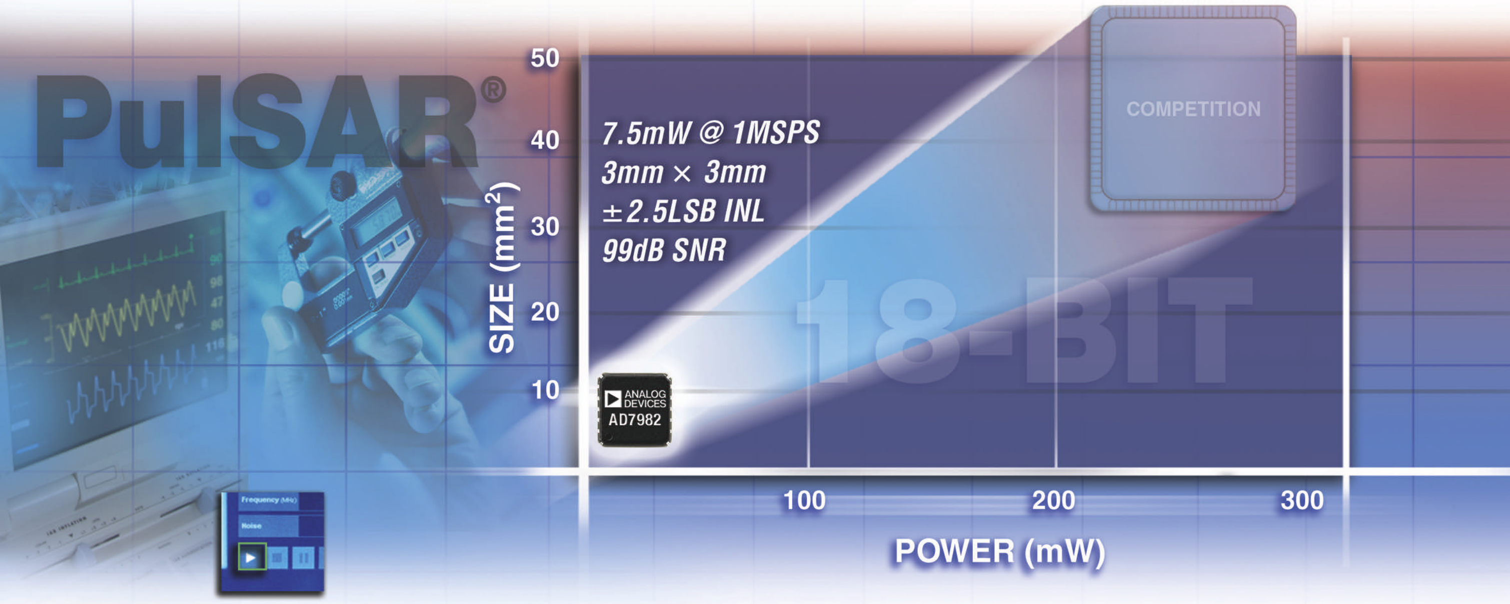

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ANALOG DEVICES

Mentor launches FPGA-synthesis tool

Mentor Graphics Inc has for more than a decade been go-ing head to head against Synplicity (www.synplicity.com) in the FPGA-synthesis market. Now, Mentor hopes to grab a greater share of that market with the new Precision RTL Plus FPGA-synthesis tool, emphasizing that the company's synthesis offerings are FPGA-vendor-independent. The company first offered Leonardo and then followed that line with Precision RTL, a general-purpose, FPGA-vendor-neutral synthesis tool that competed directly with Synplicity's Synplify FPGA-synthesis tool. The company a few years ago followed with a physical-synthesis version of Precision RTL. Designers would use the physical-synthesis tool after running an FPGA vendor's placement-and-routing system. With user guidance, the tool would locate critical paths in the layout of an FPGA and then find various areas from which users could squeeze performance and reduce footprint in the FPGA. Although the physical-synthesis tool helps designers get the best performance and smallest area from an FPGA, the technology is too advanced for the mainstream-FPGA-design market and is not vendor-independent.

Mentor and its competitors in FPGA synthesis have traditionally built knowledge of each FPGA architecture into their tools—a daunting and time-consuming task. For that reason, vendors favored just one FPGA vendor—Xilinx (www.xilinx.com)—over others and supported only a few devices in an FPGA family. Meanwhile, traditional RTL synthesis also has issues. "Achieving timing closure takes too many iterations [between synthesis and place and route], and each iteration can take as long as 10 hours to perform," says Daniel Platzker, Mentor's FPGA-product-line director at the design-and-synthesis division. "Users also face the challenge of how to control the mapping of HDL into dedicated resources." With Precision RTL Plus, Mentor hopes, designers will get the right mix of advanced functions, usability, productivity, and vendor neutrality.

New features of Precision RTL Plus are automatic incremental synthesis, which reduces the number of iterations and the time it takes to run each iteration, and a patent-pending technology for resource management, which maximizes the use of the dedicated resources in an FPGA. Whereas Mentor's and competitors' physical-synthesis tools typically support only one or two FPGA vendors and devices, the Precision RTL Plus incremental-synthesis engine and resource-management technology allow Precision RTL Plus to support 19 devices from Actel (www.actel.com), Altera (www.altera.com), Lattice Semiconductor (www.latticesemi.com), and Xilinx.

Unlike with FPGA physical synthesis, designers use Precision RTL before placement and routing. "We have a lot of intimate knowledge of the device resources but not necessarily to the same granularity as the previous technology," says Platzker. Instead, the tool performs several estimations to evaluate the design, a device's architectural resources, and its routing resources. Using these estimates, the tool identifies critical paths and automatically builds an optimized netlist for FPGA vendors' place-and-route tools. The tool does not perform preplacement or drive FPGA vendors' place-and-route tools. "We let place-and-route tools do what they do best: place for best performance," says Platzker. The result, he says, is 5 to 50% better maximum clock frequency over other vendors' tools, with an average improvement of 10%.

> "The automatic incremental-synthesis engine works late in the design cycle when designers require a small change for debugging or a change in the specification.

The last generation of FPGA-synthesis tools used partition-based synthesis. If a design required a change, users changed just one partition, leaving the other partitions intact. This approach has proved somewhat useful for team-based design, but it can be too complex and time-consuming for individual designers. To address this problem, the automatic incremental-synthesis engine works late in the design cycle when designers require a small change for debugging or a change in the specification. It can save as much as 60% in runtime, according to Platzker. Rather than employing a partitioned design, the tool compares requested changes with the initial synthesis run. "We are not paying attention to design time stamps, to comments, or to all kinds of changes," says Platzker. "Once we identify the changes, we start to propagate them to the rest of the design looking for the best results."

The tool collaborates with Xilinx's automatic incremental place-and-route tool. "If you use both tools together, you'll have a fully automatic design flow," says Platzker, noting that the combination can give you a threefold to tenfold productivity improvement, depending on design size and complexity. The engine also supports partition-based design for users who prefer it. The automatic incremental-synthesis engine runs on only the partitioned area, comparing the changed netlist for the partitioned area with the original and then performing the same selective quality-of-results optimizations.

Precision RTL Plus also features a resource manager to help design teams get the most from the dedicated resources in a vendor's FPGA. The tool creates a graphical representation of an FPGA's architecture and its available resources. The tool includes a cross-probing feature to locate and fix problems. Using the tool, a designer routes a critical path with negative slack into a dedicated RAM block. The designer can identify and remedy the problem with the tool by remapping the path into the FPGA fabric, essentially eliminating it as a critical path. Mentor worked with all the major FPGA vendors and some of the small start-ups to ready Precision RTL Plus for the mass market. Prices start at $27,100.

—by Michael Santarini

▷**Mentor Graphics**, www.mentor.com.

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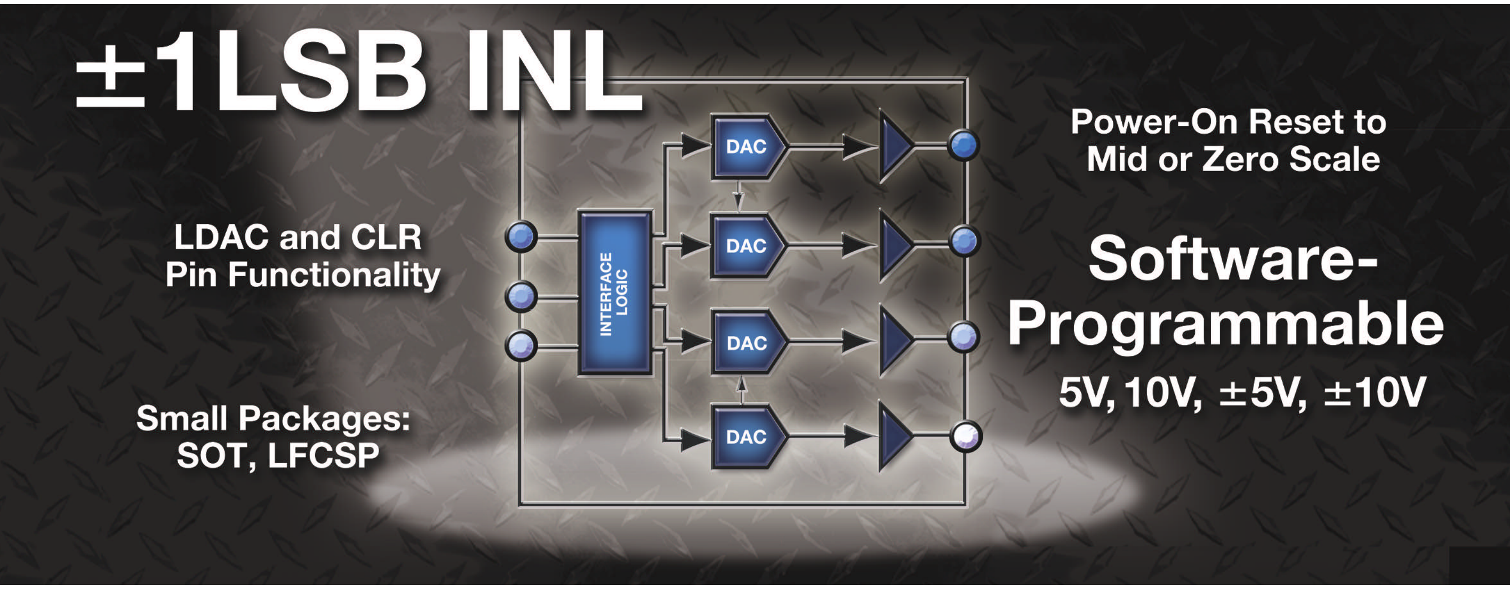

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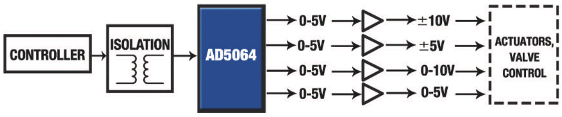

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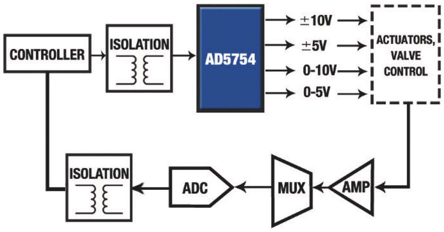

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ANALOG DEVICES

BY BONNIE BAKER

Voltage- and current-feedback amps are *almost* the same

Current-feedback amplifiers have a higher slew rate than do voltage-feedback amplifiers. As such, current-feedback amps can better solve high-speed problems than their voltage-feedback counterparts. The name "current-feedback amp" carries some mystique, but, generally, the application-circuit configurations for voltage- and current-feedback amps are the same, except for a few key points.

First, the feedback resistor of a current-feedback-amp circuit must stay within a small range of values. Lower value resistors reduce the current-feedback amp's stability. The feedback resistor's higher values reduce the current-feedback amp's bandwidth. You can find the prescribed feedback-resistor value in the current-feedback amp's product data sheet. The voltage-feedback-amp's feedback-resistance value is more forgiving. This amplifier's drive capability limits the resistor's minimum value, and the overall circuit noise limits the maximum value.

Figure 1 shows a circuit that is appropriate for either a current- or a voltage-feedback amp. If the feedback resistance, R_F, equals $2R_{IN}$, where R_{IN} is the input resistance, the closed-loop gain of each channel is −2V/V. At first glance, it is easy to assume that the closed-loop bandwidth equals the gain-bandwidth product divided by each channel's gain, or |−2V/V|. Don't make this assumption!

If you use a voltage- or current-feedback amp with the circuit in **Figure 1**, the noise gain is:

$$1+\frac{R_F}{R_{IN}/N}, \qquad (1)$$

If you add channels to the circuit, a small variation in the signal bandwidth and gain peaking in the circuit may occur.

where N is the number of input channels. This circuit's bandwidth, with a voltage-feedback amp, equals the gain-bandwidth product divided by the noise gain. For instance, if you have a voltage-feedback amp with a gain-bandwidth product of 180 MHz and there are three input channels (N=3) at a gain of −2V/V, the circuit's closed-loop bandwidth is 25.7 MHz. Additional channels reduce the closed-loop bandwidth, even though the input signals continue to see a gain of −2V/V.

If you use a current-feedback amp with the circuit in **Figure 1**, the amplifier's closed-loop bandwidth depends less on the closed-loop gain and the number of input channels. If

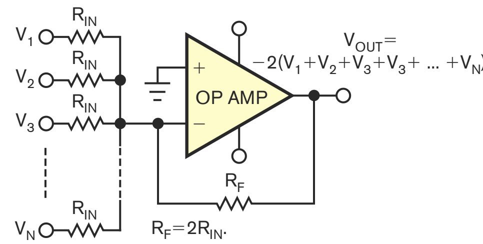

Figure 1 If you vary the number of channels in this circuit, the current-feedback amp will help keep the closed-loop bandwidth constant.

you design this circuit with such an amp, you would first pick the optimum feedback resistor, per the manufacturer's specification and the circuit's noise gain. You would then select the appropriate value for R_{IN}. From this point, if you add channels to the circuit, a small variation in the signal bandwidth and gain peaking in circuit may occur. If that scenario is a concern, go back and refine your feedback-resistor selection. For both current- and voltage-feedback amps, the noise gain always equals the result of **Equation 1**, but you can reduce the feedback-resistor value with the current-feedback-amp circuit and get an *increase* in circuit bandwidth. **EDN**

Bonnie Baker is a senior applications engineer at Texas Instruments and author of A Baker's Dozen: Real Analog Solutions for Digital Designers. *You can reach her at bonnie@ti.com.*

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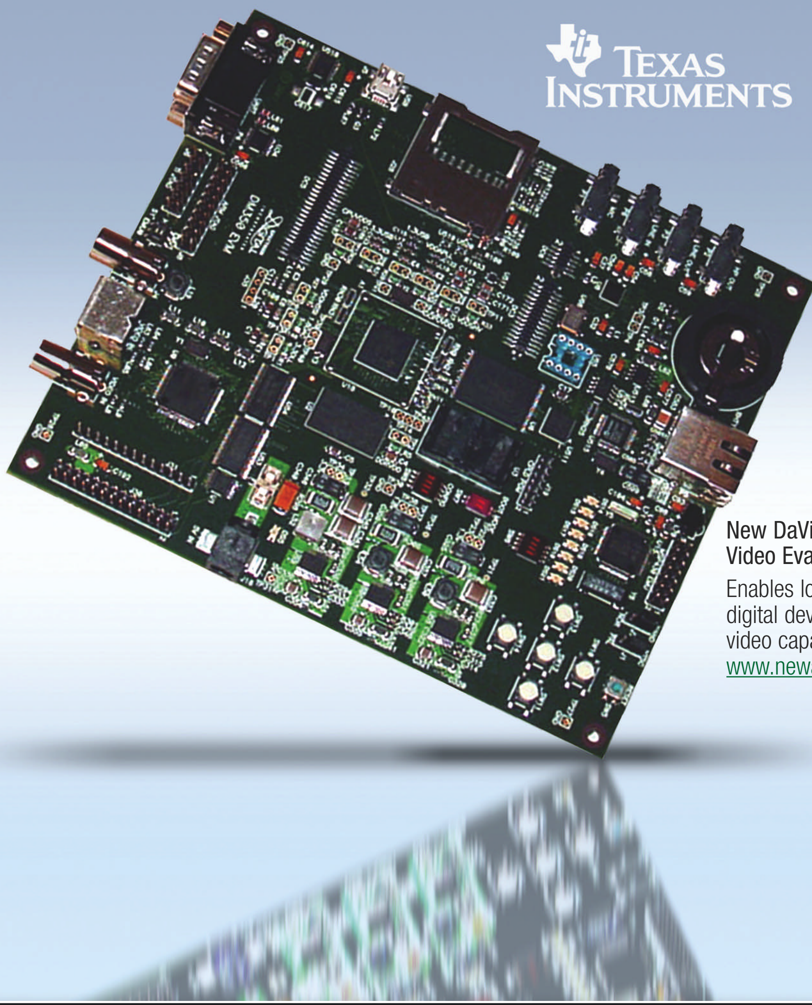

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 BY ROBERT CRAVOTTA, TECHNICAL EDITOR

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Perusing a universal remote

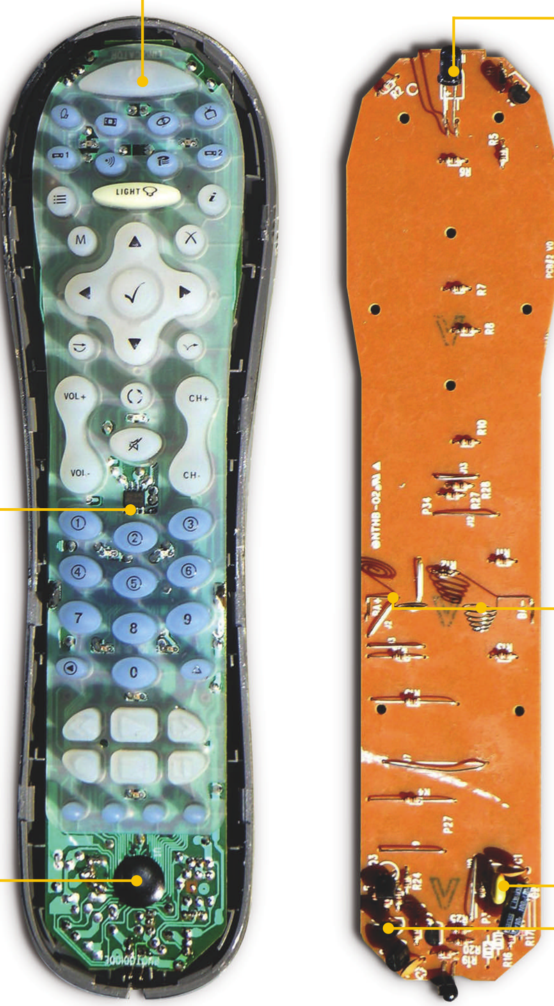
During the 1950s, Zenith Radio Corp introduced the first remote control for television. The Lazy Bones device used wires between the remote and the TV. Wireless remote controls appeared shortly thereafter, and the industry has been evolving and improving them ever since. As home-entertainment systems started to include more types of devices, such as DVD players, cable or satellite set-top boxes, and audio systems, the demand has grown to combine the separate remote controls for each of these devices into a single device.

An industrywide remote-control standard would be ideal, but such a solution seems unlikely in the immediate future. The URC (universal remote control) is an approach to help reduce the frustration of using multiple and incompatible remotes to control home-entertainment systems. This Philips Prestige SRU8015 includes many of the components that you typically find in URCs.

Using semitransparent rubber for the buttons and supporting surface enables the remote control to include backlighting for the buttons.

The infrared LED and the transistor to drive the current for the LED provide the interface to the outside world to control the electronic entertainment devices. Some remote-control schemes implement three signals to control a device's on/off state—an explicit on signal, an explicit off signal, and an on/off-toggle signal.

The EEPROM supports the learning function and allows the unit to store the user's settings even between battery changes. The learning function stores the signal transitions and timings for each button code a user "teaches" it.



These coils are battery contacts. To reduce cost, remotes may use a single-sided PCB; all of the traces are on the other side of this board.

To reduce bill-of-material costs, you can directly attach the microcontroller silicon to the PCB without packaging and covered with epoxy. The microcontroller contains a ROM instance of the infrared database; users access the database through an API that is specific to the database vendor. In this example, to access a button entry, the API needs a device-type code; a manufacturer code; and a key code, which corresponds to a row-and-column designation in the Zilog database.

Four transistors on the left side amplify the IR input from the IR photodiode that enables the URC to support learning; newer designs may use a microcontroller that includes these transistors to further reduce costs. The yellow package on the right side is a resonator to provide a low-cost clock source for the system. The electrolyte capacitor (black package) filters out the ripples and stabilizes the power in the system while the IR LED is active.

Special thanks to Zilog's Dan Mui for his insights and knowledge about designing remote controls.

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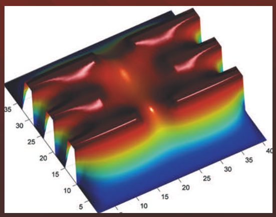

Modeling electric potential in a quantum dot. Contributed by Kim Young-Sang at HYU.

This example available at mathworks.com/ltc

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Back to fundamentals

DANIEL VASCONCELLOS

As an independent design contractor, my company faces a variety of interesting design bugs. A recent one involved a portable consumer product that included a user interface comprising a keypad, a cheap monochrome LCD, and activity LEDs. After two years of collaborative development work with our customer, the product was ready for launch.

Our customer, eager to start deliveries, was field testing his few prototypes and noticed a peculiar intermittent problem. Sometimes, nothing appeared on the LCD screen, even though the behavior of the LEDs indicated that the firmware was running OK.

We couldn't reproduce the problem in the lab. Two days later, the customer had more data. He contended that the problem happened only outdoors. Oh great, we thought—the old "works-in-that-spot-but-doesn't-in-that-other-spot" failure. Given the limited amount of observation, we wondered whether the outdoors connection might be mere coincidence. The customer speculated that the unit had a temperature problem—that the units were overheating in warm weather or in direct sunlight. So, we asked him to test the units by running them for extended periods in a hot car. He reproduced the problem, but not consistently.

We began thinking it possible that direct sunlight was overheating the liquid-crystal material and rendering it dysfunctional. We tried some outdoor testing ourselves but couldn't get the LCD to fail by leaving it out in the sun. The LCD was a complete OEM module on whose glass its maker placed the controller chip to run its pixel array, providing designers with an easy microprocessor-controllable display product. We didn't expect to have to deal with inadequacies of the LCD physics, because we are electronics designers.

A little bit of extra education provided just the insight we needed, along with some finally consistent observations from the customer. Using several units, he managed to get the same behavior from each one. If he powered them up in the sun, the units failed to show anything on the LCD. If he powered them up while shading the LCD screen, *they booted fine*! Our educated theory? Somehow, sunlight reached some part of the controller chip, and a photoelectric effect of intense light hitting the chip-on-glass assembly was causing the silicon to malfunction, but only during its power-up cycle. It sounded far-fetched, but we consistently confirmed the behavior. Now, we needed a solution. And our customer had already shipped some of his first production units and was dreading the returns.

Fortunately, the LCD module had a software-reset command. We tried using it on software start-up. Occasionally, it worked, but occasionally wasn't good enough. We then found that a brute-force loop of some 50 or so reset commands to the LCD-controller chips eventually brought around any that were failing to start up properly in the sunlight. Luckily, we had designed the product's firmware for an easy field update, so we solved the problem for production and for the already-delivered units. It seemed pretty kludgy to us, but it always worked, and, in real time, it moved too fast for anyone to notice it.

Remember: Your engineering education began with fundamental science for good reasons. It helps you understand real-world problems, because chips and software aren't always pure electronics-theory Tinkertoys that snap together and just work. And make sure beta-testing happens and that the users are good observers, with at least a little sense of scientific method. EDN

Design Engineer Chris Lee is one of the founders and owners of Cheshire Engineering Corp. Like Chris, you can share your tale and receive $200. Contact Maury Wright at mgwright@edn.com.

Rarely Asked Questions

Strange but true stories from the call logs of Analog Devices

Contributing Writer James Bryant has been a European Applications Manager with Analog Devices since 1982. He holds a degree in Physics and Philosophy from the University of Leeds. He is also C.Eng., Eur.Eng., MIEE, and an FBIS. In addition to his passion for engineering, James is a radio ham and holds the call sign G4CLF.

Op-Amp Noise Can Be Deafening, Too

Q. Last month you blamed op amp noise on external resistors. Surely this is not always the case?

A. By no means. Resistor noise is a common problem, and is often overlooked, but op amps themselves can be noisy too.

An op amp has three noise sources: voltage noise (V_n) across its inputs and current noise (I_n) in series with each input.

V_n can be as low as 900 pV/√Hz for op amps with bipolar junction transistor (BJT) inputs; amplifiers with JFET inputs can have around 2 nV/√Hz, but must use large devices with large input capacitance (~20 pF). Digital CMOS is noisy, which is why early CMOS op amps had a poor reputation for noise, but modern analog CMOS processes can make op amps with noise of 6 nV/√Hz.

JFET and CMOS op amps have very low I_n, though. Some electrometer types have I_n as low as 0.1 fA/√Hz, but values in the range 10 to 50 fA/√Hz are more common. Bipolar op amps have much higher current noise — up to several pA/√Hz for wideband types.

In low impedance circuits, I_n does not matter. In high impedance circuits, on the other hand, even a small I_n will produce a large noise voltage. So, for high impedance applications, we must choose op amps with low I_n. If, however, we require very low noise, we must choose op amps with low V_n and use low impedances. In the middle impedance ranges, as we saw last month, the thermal noise of the resistors dominates.

Over most of their frequency range, op amps have white (constant spectral density) noise, but at low frequency the noise rises at 3 dB/octave from the "1/f corner frequency." So, if low noise at low frequency is required, we must consider the 1/f corner as well as V_n and I_n. This requires us to choose a value compatible with our operating frequencies.

When op amps were new, "popcorn noise" was a serious issue that resulted in random discrete offset shifts in a timescale of a few tens of milliseconds. This made a noise like cooking popcorn if sent to a loudspeaker. Some devices were so badly affected that, in the words of an engineer affected by the problem, "You could measure it with a frog's leg and a stopwatch."[1] Today, although popcorn noise can still occasionally occur during manufacturing, the phenomenon is sufficiently well understood that affected devices are detected and scrapped during test.

This is too complex a topic for a short RAQ; visit the link for a more detailed discussion.

[1] *This refers to Alessandro Volta, after whom the volt is named, who in 1791 observed that electrical currents applied to the legs of a recently-killed frog made them twitch and used the phenomenon to detect electricity.*

To learn more about noise,
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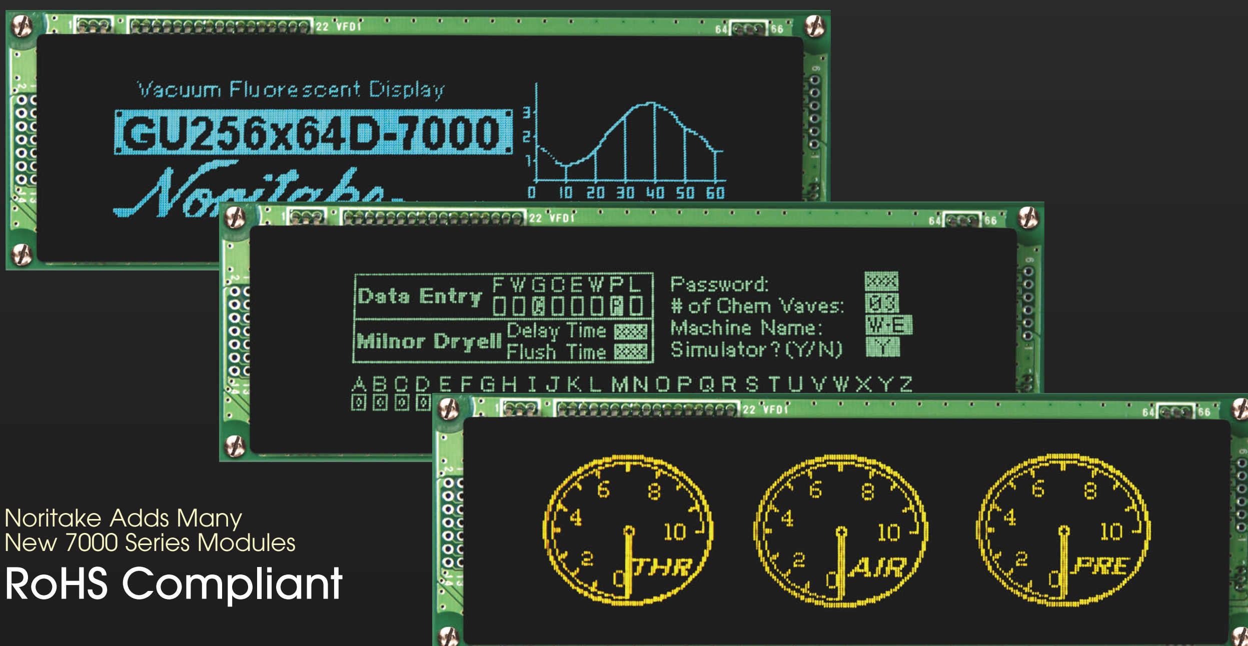

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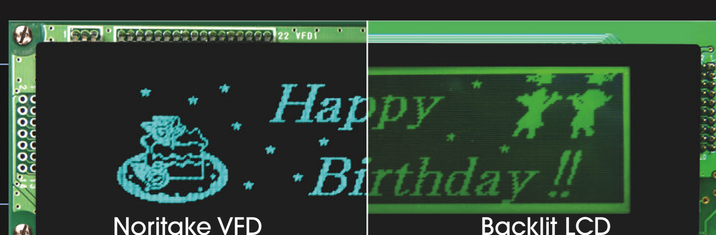

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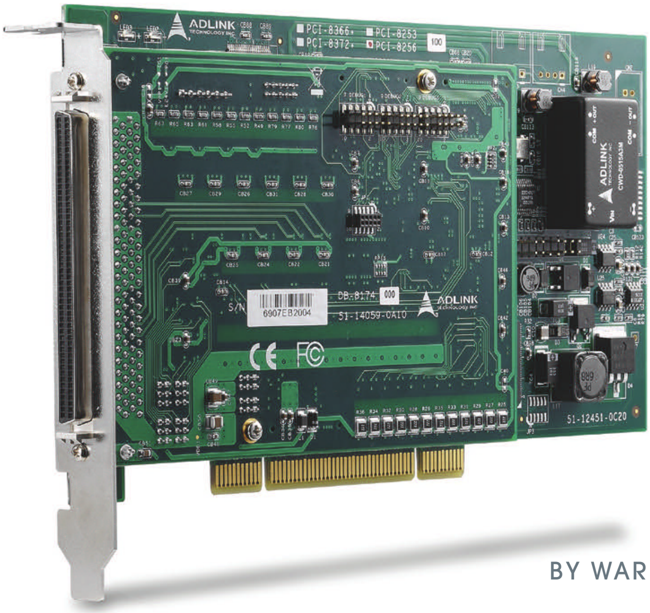


Figure 1 The Adlink PCI-8174 is an off-the-shelf stepper and servo controller for multiaxis, time-critical motion sequences.

AS NEW DESIGNS COMBINE ELECTRONIC CIRCUITRY, MECHANICAL ACTUATORS, AND MICROPROCESSOR SOFTWARE, A GROWING PERCENTAGE OF EMBEDDED DEVELOPMENT FALLS UNDER THE RECENTLY REVIVED "MECHATRONICS" MONIKER.

BY WARREN WEBB • TECHNICAL EDITOR

MECHATRONICS-BASED embedded design

With fully interactive products now the norm, mechanical-control circuitry has emerged as an integral part of embedded-system design. Although designers have since the early days of electronics used electromagnetic-control circuits to energize motors, relays, solenoids, and speakers, today's "smarter" motion-control components replace traditional mechanical elements with microcontroller-based circuitry to improve accuracies and coordinate movements. This trend brings traditional embedded-system design close to the newly coined "mechatronics" methodology, which combines mechanical, electrical, control-system, and embedded-software design.

Engineers at the Japanese company Yaskawa conceived the term "mechatronics" almost 40 years ago, yet people have until recently rarely used the term. Although a simple electromechanical circuit might meet the broadest definition of mechatronics, proponents prefer to apply the term to projects requiring a much higher level combination of disciplines, including electrical-circuit design, computer-aided-machine design, digital-control systems, and real-time-computer software. This new interest has sparked a number of leading universities to offer course work and even engineering degrees in mechatronics methodology. For example, North Carolina State University and the University of North Carolina offer a joint curriculum leading to a bachelor's degree in engineering with a mechatronics concentration.

Mechatronics offers a system-level approach to system design that reduces product-development times and risk through the use of simulation, computer-aided design, virtual prototyping, and design-tool integration. Mechatronics techniques allow designers to accurately simulate the performance of a machine early in the design process to ensure that the machine meets requirements and customer expectations. Unlike traditional electromechanical-system development, the virtual-simulation objectives of mechatronics tools provide the potential for simultaneous development of mechanical, electrical, and software elements. Automatic tools on the horizon promise to extend the control-system design from mostly trial and error to optimization through simulation. Mechatronics does require a substantial learning curve and time investment in system modeling that most embedded motion-control projects would not otherwise require.

AT A GLANCE

- To provide a more realistic interaction with the user, embedded-system designers are adding controlled mechanical motion to their products.
- Emerging mechatronics tool sets promise to integrate the electrical, mechanical, control, and embedded-software disciplines.
- Mechatronics tools allow designers to simulate the performance of a machine early in the design process to verify requirements.
- Product modeling and virtual prototyping shorten design cycles because electrical, mechanical, and software teams can work in parallel.
- Off-the-shelf motion-control boards and development kits provide an easy way to integrate mechanical devices with embedded-system applications.

Engineers may employ advanced mechatronics techniques for complex designs; in these designs, multiple motors or actuators coordinate to control precise motion. However, the fundamental motion-control principles remain intact. For example, dc motors find wide use in applications requiring servo control of rotational speed or torque. The basic relationships are that motor speed is proportional to the applied voltage, and output torque is proportional to the current. The designer's task is to pick the operating speed and then provide enough drive current to match the required load torque. The control problem becomes more of a challenge when you must control the speed of the dc motor during operation. The most popular approach to efficient dc-motor operation is to apply a PWM (pulse-width-modulated) square wave with an on-to-off ratio corresponding to the desired speed. The motor acts as a lowpass filter to translate the PWM signal into an effective dc level. PWM-drive signals are popular because a microprocessor-based controller can easily generate them. Stepper motors are also popular embedded-motion-control devices because they move in discrete steps, provide accurate angular-position information, and are relatively easy to control. The rotor of a stepper motor is made of permanent magnets arranged in a series of poles that determine the step size. The stator includes multiple windings to create a magnetic field that interacts with the rotor's permanent magnets. As a sequence of pulses from a control circuit turns the stator windings on and off, the motor rotates forward or in reverse.

Mechanical add-ons are finding their way into many traditionally all-electronic embedded-system applications. For example, users often complain that touchscreens are more difficult to use than physical buttons because of the lack of tactile feedback. Designers have responded with audio and visual clues, but these clues alone do not match the positive feel of a mechanical pushbutton. Immersion provides a new alternative with its TouchSense system that promises to transform conventional, passive touchscreens into active displays with graphical buttons that press and release like pushbuttons. The TouchSense system supplies fast tactile response synchronized with sound and graphical image changes and does not affect touchscreen performance. You can add it to flat touchscreens as large as 6 in. diagonal and apply it to most touchscreen-sensing technologies, including capacitive, resistive, surface acoustic wave, and infrared. A software tactile-effect library controls a small electromechanical actuator, like the vibrator in mobile phones, which provides the physical movement.

To support the growing popularity of embedded systems with mechanical components, a wide range of board-level manufacturers offer off-the-shelf, plug-in motion-control boards for standards such as PCI, CompactPCI, PC/104, and VMEbus. These boards allow designers to add motion control to a PC or an embedded system without digging into the details of controller design or feedback-loop optimization. For example, the Adlink Technology PCI-8174 low-cost stepper- and servo-motion-control card for the PCI bus offers an onboard DSP for simplified implementation of time-critical motion sequences (**Figure 1**). This board finds use in applications such as semiconductor-manufacturing equipment, electronic assembly, optical-inspection equipment, vehicle simulators, and precision carving machinery. The multiaxis-operation design of the PCI-8174 allows linear interpolation using all four axes and circular interpolation using any two axes. With the DSP onboard design, the PCI-8174 can also support firmware customization. The PCI-8174 is available now at prices starting at $1190.

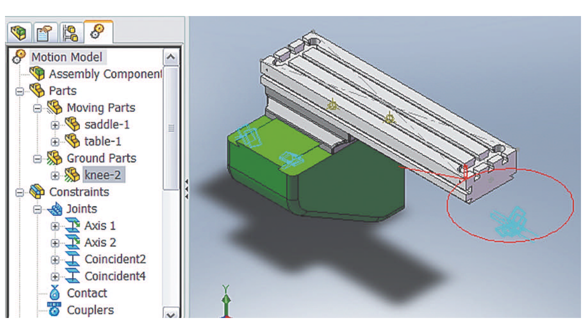
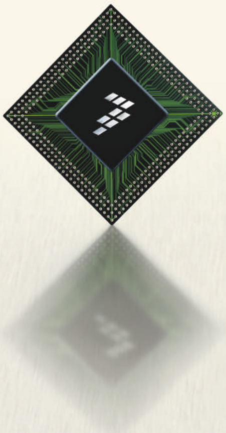


Figure 2 National Instruments' LabView and SolidWorks' CosmosMotion provide a closed-loop simulation of the dynamics of an electromechanical system.

CONTROL KITS

If the objective is to rapidly integrate motion into an embedded product, the easiest way to get started is with an off-the-shelf development kit. For example, the MCK2812 DSP motion-control kit from Technosoft is a popular evaluation platform for investigating both the hardware and the software aspects of dc motors. This kit includes a Texas Instruments TMS320LF2812 DSP, 128k words of program RAM, and a serial-communications interface, all on a small PCB (printed-circuit board). The kit also includes an inverter power module and a brushless motor equipped with Hall sensors and a 500-line encoder for direct experimentation. All communication between the host PC and the DSP board is through a flash-resident communication monitor with downloading, debugging, and inspection functions. It includes a set of ready-to-run examples with assembly source code. The kit also features the DMCD (Digital Motion Control Development) software platform with an in-



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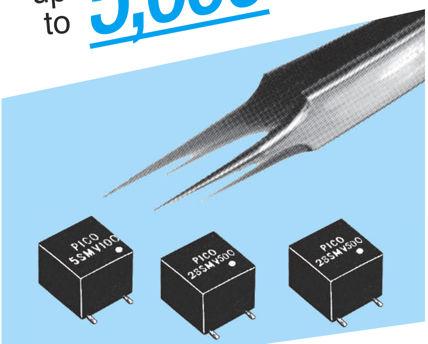

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tegrated debugger, a basic assembler, a linker, and other facilities that allow you to create, modify, and test assembler applications within a project-management system. The MCK2812 DSP motion-control kit costs $3290 and is available directly from Technosoft.

Mechatronics engineers often determine operational behavior and uncover system shortcomings by detailed, upfront modeling and simulation of proposed designs. Engineers can exercise an accurate system model before the availability of physical hardware to determine whether the system meets specifications and customer expectations. Unfortunately, the required modeling process is unduly complicated when mechanical and electrical elements coexist. One solution to this problem is to extend a modeling language to cover hybrid systems. The IEEE took this approach by extending the VHDL (very-high-level hardware-description language) with AMS (analog/mixed-signal) extensions. The IEEE built the language, informally known as VHDL-AMS, on the IEEE Standard 1076-1993 language, and it allows designers to develop and simulate analog and mixed-signal models.

Mentor Graphics' SystemVision development tool uses the VHDL-AMS language as its foundation to describe the behavior of hybrid hardware technologies typically in embedded mechatronic systems (**Reference 1**). These systems contain a combination of analog, digital, and electromechanical components, each requiring significantly different modeling techniques. SystemVision allows designers to include components of different levels of abstraction within the same system model to focus on the details of a part of the system and maintain its context within the overall system design. Designers can use VHDL-

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THE REQUIRED MODELING PROCESS IS UNDULY COMPLICATED WHEN MECHANICAL AND ELECTRICAL ELEMENTS COEXIST.

AMS signal-flow models in high-level block diagrams, and, as the design progresses, they can incorporate physical-hardware models into the system model to successively verify proper system performance. They can use algebraic or differential equations to describe a system model that incorporates a combination of various technologies, such as mechanical, magnetic, hydraulic, or thermal effects. For example, designers can use a three-phase design tool from Infolytica to create a VHDL-AMS model of an automotive alternator.

HYBRID SIMULATION

National Instruments and SolidWorks have teamed up to bring electrical and mechanical modeling and simulation to mechatronics designers on a grand scale. The alpha version of their recently released Mechatronics Toolkit allows designers to simulate the integrated mechanical and control design in software before moving to the prototype and production stages. Designers can simulate mechanical dynamics, including mass and friction effects, cycle times, and individual component performance before specifying a single physical part. They can tune and customize control-system and feedback elements entirely through the software model. They can test electrical performance and real-time response times at operational extremes without stressing a part. When they move the design from prototyping to production, they can reuse the same software that they used for simulation.

The Mechatronics Toolkit integrates several graphical-design packages with software linkages to transfer parameters between the electrical and the mechanical environments. SolidWorks, a popular mechanical, 3-D-computer-aided-design program, includes tools for mechanical design, verification, motion

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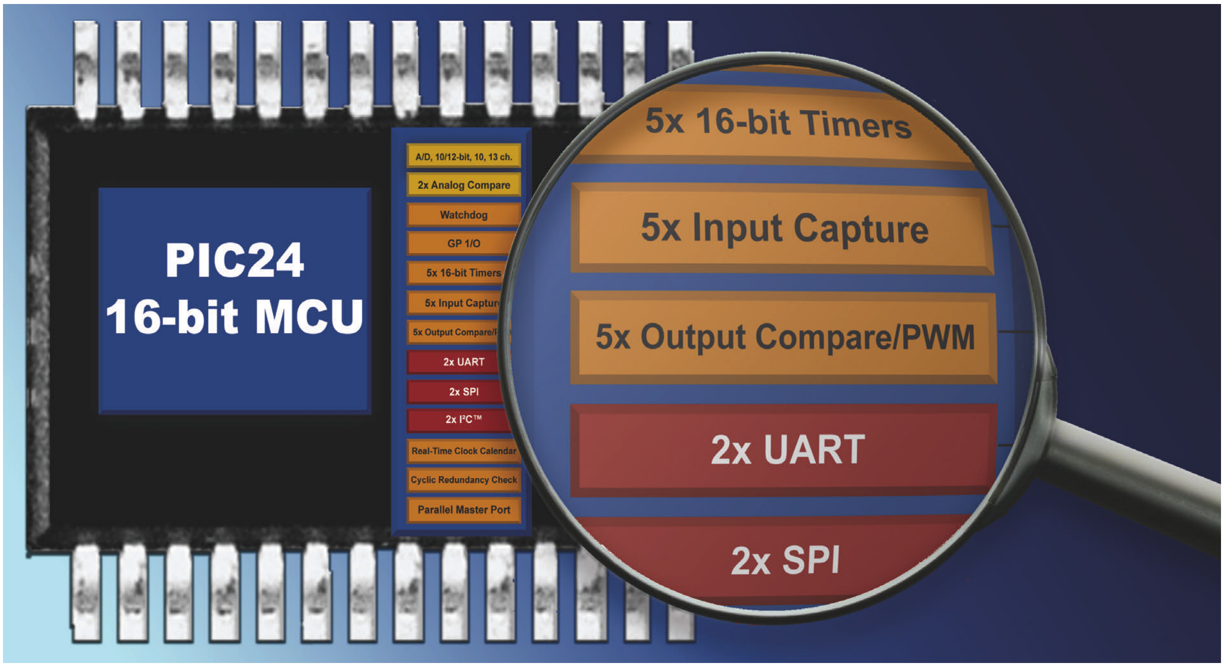

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simulation, data management, and project communications. CosmosMotion, a SolidWorks add-on for virtual prototyping, uses mechanical dynamics to help simulate mechanism motion. National Instruments' LabView provides the tools for electrical and control-system design, simulation, and automatic code generation. This combination of LabView for a control-design environment and SolidWorks/CosmosMotion for a mechanical-design environment provides designers with a true closed-loop simulation of the dynamics of a mechanism and the controls that act on it (**Figure 2**). National Instruments offers a free mechatronics resource kit that demonstrates how these tools can integrate mechanical design, control design, simulation, sensing and actuation, signal processing, and electronic design (**Reference 2**).

All of these tools and techniques demonstrate an industrywide effort to improve electromechanical development by streamlining design, prototyping, and deployment. The latest mechatronics technologies promise to deliver higher profits through low-risk, low-cost development and increased efficiency. To take advantage of these benefits, designers must adopt a new design strategy that relies on graphical modeling and system simulation. These tools have the potential to greatly shorten the development cycle and even to eliminate the need for some of the project engineers or software developers. The industry now has the graphical tools to model a proposed system, automatically reconfigure an off-the-shelf FPGA with microprocessors and custom circuitry, optimize the mechanical control circuitry, and then synthesize the needed software. Maybe the next generation will eliminate the need for an engineering staff altogether. EDN

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2. Mechatronics Resource Kit, National Instruments, http://digital.ni.com/express.nsf/bycode/exg9gi.

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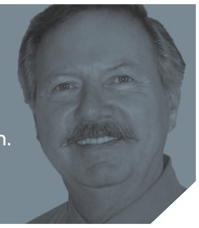

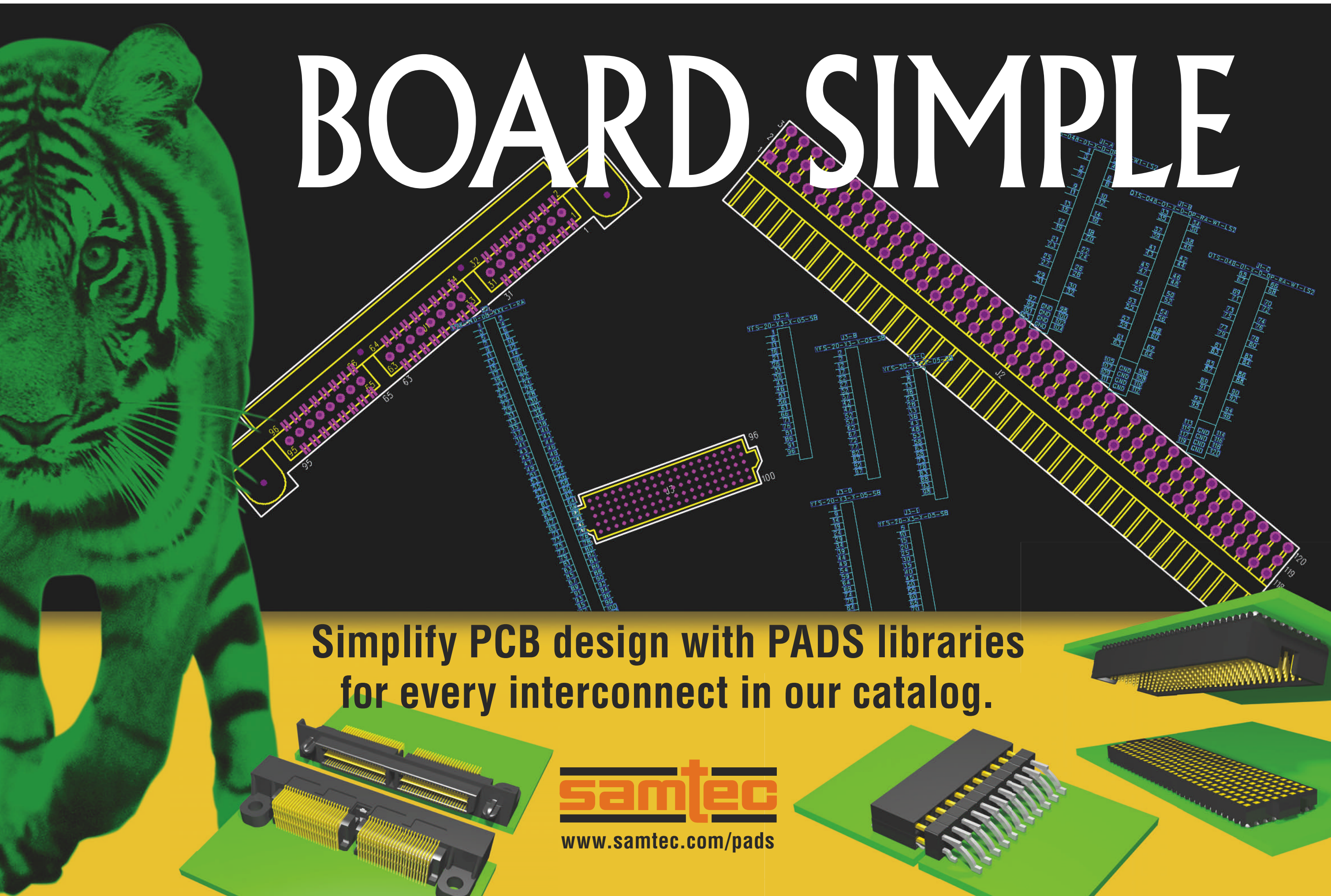

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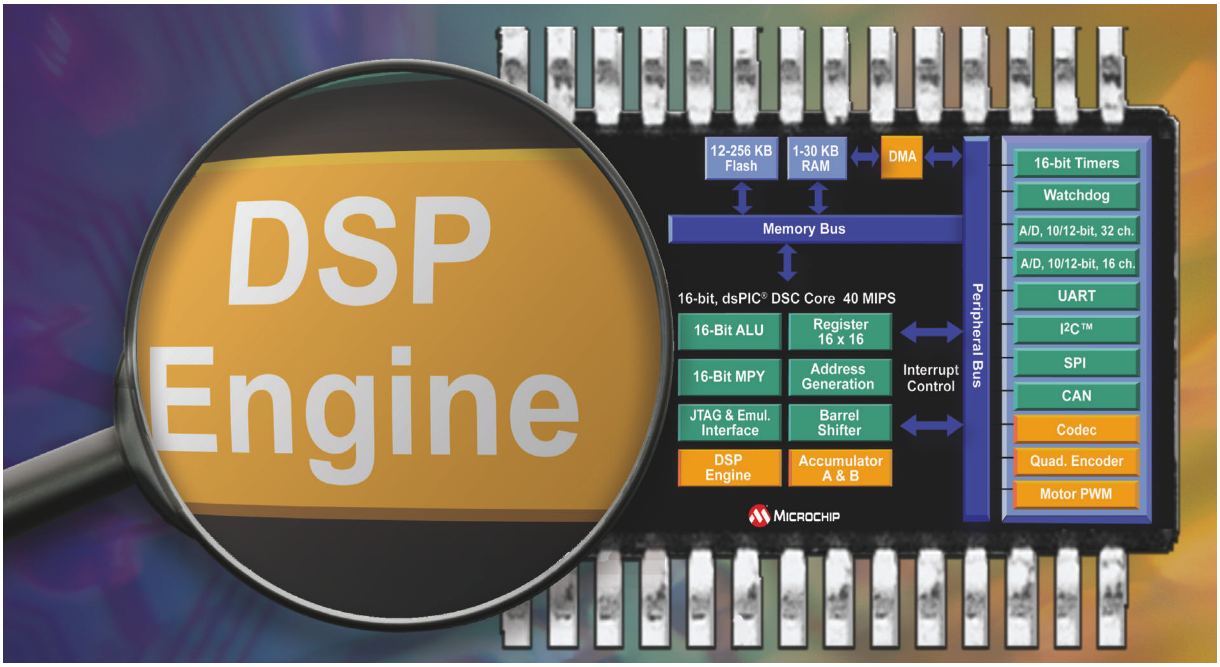

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BY PAUL RAKO • TECHNICAL EDITOR

You would think that selecting operational amplifiers would be easy. After all, they have only three important pins: two inputs and one output. In designing a typical op amp, however, you must also consider the two power pins, and this total of five pins has a bewildering array of specifications. Given that fact, amplifier design and selection can be among the most daunting tasks that analog-system engineers face.

SELECTING OP AMPS

SELECTING OPERATIONAL AMPLIFIERS CAN BE AS COMPLICATED AS THE SPECIFICATIONS FOR THESE PARTS. BY UNDERSTANDING THE BASICS, KNOWING YOUR APPLICATION, AND USING STANDALONE AND ONLINE TOOLS, YOU CAN MAKE THE RIGHT CHOICE.

In selecting an amplifier, you must determine the maximum and minimum voltage for the part's operation, its quiescent current, the current the op amp must deliver to the load, and any other current it uses. You might, for example, set up the two power pins for bipolar operation on split supplies or for single-ended operation by hooking the negative power pin to ground (**Figure 1**). Although you can connect any amplifier in a bipolar or single-ended circuit, other factors often make the part suitable for single-ended operation. In addition, the input pins almost always include ground in their input range or provide for rail-to-rail inputs, in which the input pins can operate at either extreme of the power-supply voltage. Further complicating the design is the fact that op-amp data sheets typically express specifications for single-ended operation, despite the possibility that a test engineer could change the part's operating conditions and restate the specs to reflect bipolar operation.

The output current is a key spec. Rail-to-rail-output parts provide usable drive current even when the output pin is less than 0.6V from either power-supply rail. Parts that use FET outputs can swing closer to the rails than parts with bipolar outputs. For example, the Intersil 30-mA EL5020 can swing to within 15 mV of either rail at 5 mA. To ensure accurate, low-distortion performance, you must also understand output-pin impedance, which varies with frequency. In addition, the output pin must drive some level of capacitive loads. Some parts, such as National Semiconductor's LM8272, drive unlimited capacitive loads, whereas typical video amplifiers oscillate with just tens of picofarads of load capacitance.

Dave Kress, director of applications engineering for Analog Devices, sees five important elements in amplifier selection (**Figure 2**): bandwidth, power supply, the requirement for multiple parts in a package, application, and cost. On the other hand, Tim Green, linear-applications manager at Texas Instruments' Burr-Brown division, narrows down the criteria to three: voltage, current, and bandwidth.

However, Paul Grohe, an applications engineer at National Semiconductor, thinks more about the inside of the amp. "Bias current and bandwidth—the two Bs—are what matters," he says. "A fast part will use more current, and a low-noise part will use more current. And, if you have a high source impedance, the input-bias current is the most important spec."

Bob Pease, staff scientist at National Semiconductor, in a jab at the company's competitors, notes that the spec doesn't matter if the supplier can't deliver the parts on time. He also says that noise is an often-overlooked, yet critically vital parameter. "There are no easy answers; you have to use your judgment," he says. "In every application, there are one or two key parameters, and you have to figure out what they are. You can't have everything."

Tim Regan, application manager for Linear Technology's signal-conditioning unit, uses the acronym SNAP (supply voltage and current/need for ac or dc performance/amplifier count/packaging) to help engineers remember the important trade-offs. Patrick Long, business-marketing manager for op amps and comparators at Maxim, also mentions packaging as an important criterion. If the part targets cell phones, for example, you would want to use a flip-chip or solder-bump package. These ultrasmall packages provide high performance analog functions with a board area the size of a silicon die.

One way to understand the scope of selecting an op amp is to look at the structure of the data sheet. The first page is a valuable tool that reveals key features and the intended application. By ignoring marketing adjectives, such as "slow" and "fast," and looking for the actual speed figure, you can quickly see whether the amplifier is in the right ballpark for your application. The first page may describe the process that the manufacturer used to make the op amp (see **sidebar** "Op-amp processes").

A section on absolute-maximum ratings typically follows the first page in an op-amp data sheet. This section always covers the highest voltage and temperature that you can subject the part to. It should be obvious from the prominence of this section that these parameters are critical in your selection because they are absolute-maximum values. The part cannot exceed these limits for a nanosecond.

Data sheets also include tables on dc and ac performance and on operating voltage. The tables clearly state the operating voltage that the part was running on when the designers created the tables. The first page may claim that the part works at voltages as low as 2.7V, yet the tables may show that the part can run at 3V. Although it may be acceptable to run a 3V part at 2.7V, you cannot use the specification in the 3V-data-sheet table. Either you have to ask the manufacturer to characterize the part at the lower voltages, or you have to do it yourself. The values in the tables are contractual obligations that the manufacturer must meet.

Pages of charts follow the tables in the data sheet. Although these charts do not represent a legal obligation, they are important. For example, the tables may claim a huge PSRR (power-supply-rejection ratio), whereas the charts show that this specification decreases drastically with increasing frequency. If an amplifier is operating from a 1-MHz switcher that has a 1-MHz output ripple, you must evaluate the PSRR at 1 MHz from the appropriate chart and remember that designers created the chart at a certain operating voltage that may produce more beneficial results than your circuit will produce. Similarly, the tables base voltage noise on the flat-band noise at higher frequencies. For dc or low-frequency applications, you must con-

AT A GLANCE

- All five pins of an amplifier have important specs.
- The application often drives the selection process.
- Understand the data-sheet sections to better choose parts.
- The semiconductor process affects amplifier specifications.
- Online tools and selector guides can help you find the right part.
- Consider using specialty amplifiers.

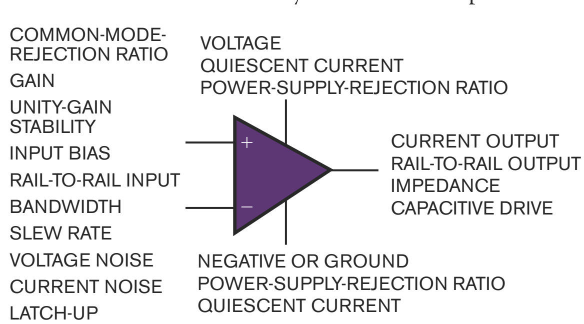

Figure 1 An op amp has only five pins, but each has a variety of specifications.

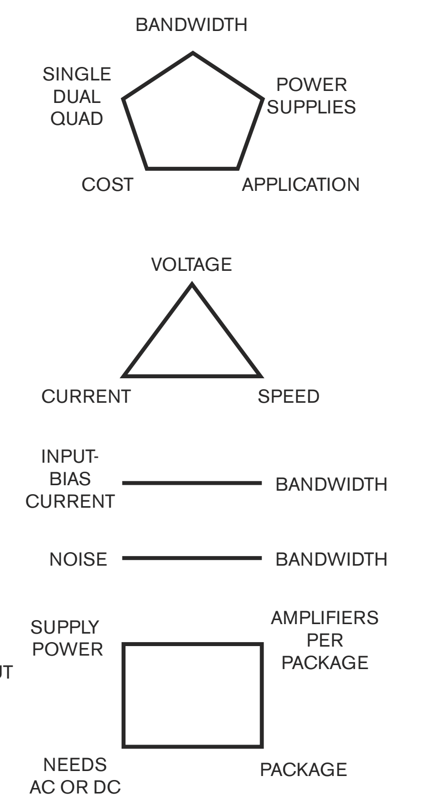

Figure 2 There are many ways to look at the trade-offs in selecting an op amp.

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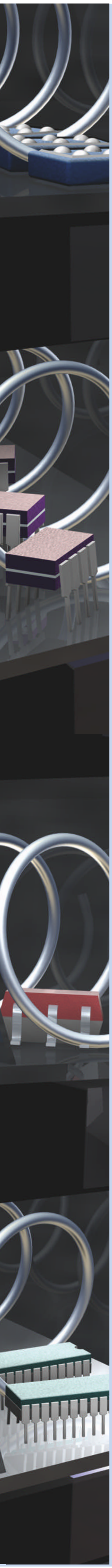

OP-AMP PROCESSES

Some amplifier manufacturers think that you should judge a part purely on its specifications without worrying about the process that went into its manufacture. Although this attitude has some validity, almost every IC designer and application engineer must consider the semiconductor process as well as the specs. Doing so helps them to broadly categorize their parts and to make certain assumptions about the specifications.

The original process that manufacturers used was bipolar, employing conventional transistors rather than FETs (field-effect transistors) or MOSFETs (metal-oxide-semiconductor FETs). Using bipolar processes means that the part can operate on higher voltages and is generally faster. Bipolar transistors have higher transconductance, easing design. If you use an isolated process, the design can work at much higher frequencies because the internal stray capacitance is often one-tenth that of a conventional process. This type of process often uses dielectric isolation, meaning that each transistor is in its own glass-isolated bowl. Some processes are only trench-isolated, meaning that the side of the transistors is glass-isolated but the bottom is junction-isolated as in a conventional bipolar process. The speeds for trench-isolated parts are better than those for plain bipolar but not as good as full dielectric isolation. The approach also prevents latch-up, in which the substrate forms a parasitic SCR (silicon-controlled rectifier). Because the parts do not latch up, you can exceed the common-mode range and have voltage at the inputs before you apply power to the part. Like all things analog, there is a downside to dielectric isolation, even beyond its greater cost. The glass walls around all the transistors have 10 times lower thermal conductivity than with junction isolation. As a result, designers rarely use dielectric isolation for higher output-current amplification.

The other broad category of amplifier process is CMOS (complementary metal-oxide semiconductor). CMOS parts cost less because their manufacture involves fewer process steps. CMOS parts also usually have low operating current. One of the best features of CMOS is that it requires a minuscule amount of input-bias current on the input pins. For example, Texas Instruments' CMOS OPA2355 has 0.05 nA of input bias, second only to JFET (junction-FET)-input parts. CMOS parts are usually 5V parts, although some 12V CMOS processes exist. Because early CMOS parts took advantage of the low operating currents of CMOS, the parts exhibited voltage noise–not an inherent property of CMOS but rather a design decision to use low bias currents and small transistors in the input section. For example, National Semiconductor manufactures its LMV751 in CMOS, but it has low voltage noise because its designers used large input transistors and higher quiescent current in the input-differential-transistor pair. Another process, BIMOS (bipolar MOS), includes both bipolar and CMOS transistors.

The less popular but still-useful bipolar-JFET process adds mask steps to allow the creation of JFETs. Like CMOS transistors, the JFETs have low-input-bias current. Older JFET parts, such as National Semiconductor's LF411 and Analog Devices' AD549, provided low bias current before CMOS parts became prevalent. TI offers modern JFET parts that provide low bias current but are also fast. The TI OPA656, for example, has a bandwidth of 500 MHz. JFETs also have lower input-voltage noise than CMOS transistors because diffusions in the wafer substrate bury the JFETs. In contrast, CMOS transistors sit on the surface of the die where they are subject to the lattice defects and crystal impurities that cause noise. Again, this approach involves a trade-off: Diffusion during manufacturing controls the JFET parameters. CMOS-transistor properties depend more on lithography in manufacturing. Thus, CMOS parts have better input-pair matching, lower offset voltages, and less drift.

When an application requires higher speed than bipolar parts can provide, designers can turn to SiGe (silicon-germanium) processes. The higher electron mobility in the base area, thinner base regions, and higher emitter-current density of these processes give op amps bandwidths that exceed 1 GHz. The parts use more current and have the same stability issues as all other high-speed parts. SiGe processes are seeing use in differential-input amplifiers for high-speed ADCs and high-speed communications amplifiers.

Other processes include GaAs (gallium arsenide) and SOS (silicon on sapphire). The GaAs process is blazingly fast, with even higher electron mobility and thinner base regions than SiGe. The downside is that GaAs, unlike silicon, uses no easily formed insulating oxide. Silicon oxide is glass and can isolate different layers of metallization. Without this process feature, GaAs trails the silicon process but provides parts operating at 10 GHz and higher. Prices and operating currents are higher, as well. In SOS-process technology, the dielectrically isolated transistors are fast, just as in an oxide dielectric-isolation process. Because the transistors are isolated with sapphire instead of glass, however, the thermal conductivity is that of a crystal; glass, in contrast, has low thermal conductivity. SOS parts are thus fast and provide lots of power output. Manufacturers can build them with CMOS-process flows that have fewer mask layers than bipolar processes do.

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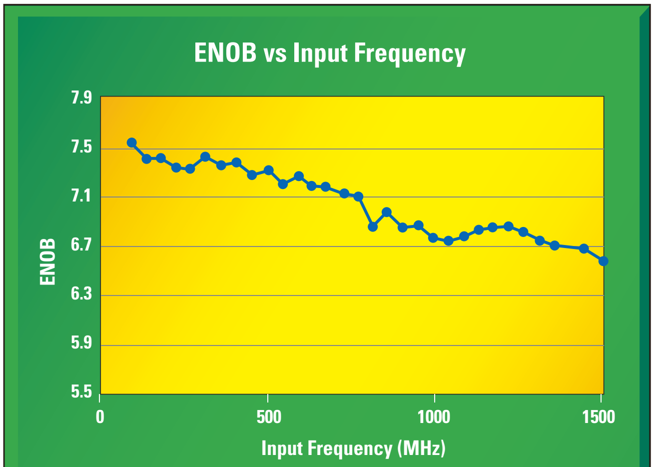

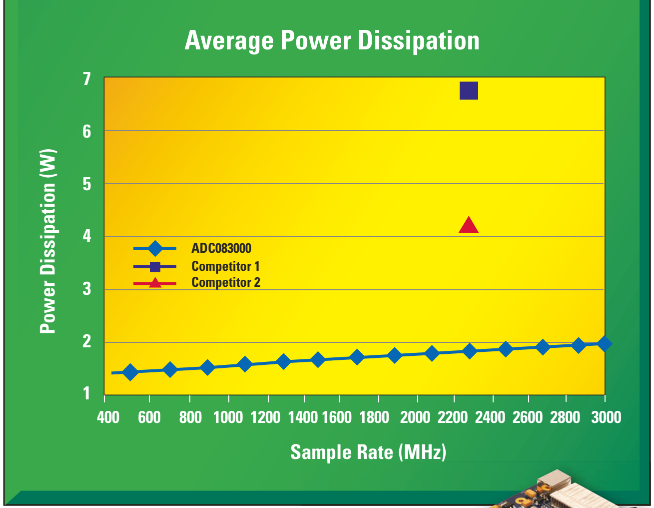

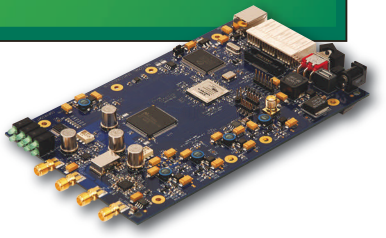

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sult the charts to determine the noise in your circuit's frequencies of interest (**Figure 3**).

Examine every chart and think of what your fellow engineer who measured the data is trying to tell you. Often, your fellow engineer at a semiconductor company includes a chart that highlights a less flattering specification of an amplifier. If a chart shows that an amplifier has 90% overshoot at 10 pF of output capacitance, the part is subject to instability.

The general description and application section follows the chart section of a typical data sheet. In this section, you can learn of appropriate applications and read about any peculiarities or special features of the amplifier. The application section may warn you that the part will burn up if you overdrive the outputs. In some older parts, the application section may warn that the part exhibits phase reversal—that is, when you bring the input pin past its common-mode range, the output of the amplifier suddenly inverts, even though the inputs never cross zero.

The part number, or suffix, section of the data sheet may be toward the end, but some manufacturers, such as TI, put this information on the front page. Every package and voltage rating of the part gets its own part number. The manufacturer may also include numbers for lead-free ROHS (restriction-of-hazardous-substances) parts. Part numbers also differ for parts in a rail or in a 4000-part reel. It is exasperating to lay out a board with a different package from the one you intended because you used an incomplete part number. Errors such as these can cost weeks or months in the development cycle.

One of the last sections of the data sheet is often the packages section, which includes drawings and suggested PCB (printed-circuit-board) patterns. If your PCB has a low profile, the overall height of the package may be the critical performance specification you must meet.

ONLINE TOOLS CAN HELP

Never hesitate to call the local field-application engineer or the factory-applications group. Analog Devices and Texas Instruments sell almost every type of op amp, so they have no reason to steer you to a specific part. One exception to this rule is that manufacturers often want to promote their newest parts in the hope of recovering the costs of designing them. For this reason, National Semiconductor's Grohe likes to use selector guides. "A parametric search will return all the parts that meet your required specifications, whether the part was designed yesterday or 20 years ago," he says. Grohe developed the downloadable selector guide you can get from the company's amplifier Web page. TI, Analog Devices, STMicroelectronics, and others also provide online selector guides.

Linear Technology developed another helpful, free, fully functional, downloadable tool, LTSPICE, which Mike Engelhardt designed. He assures that the program converges, even with magnetic elements. Texas Instruments also offers the downloadable, node-limited, fully functional Tiny TI SPICE program, which provides accurate results when you use it with accurate models. Analog Devices' Web site also has a downloadable simulator and the ADIsim op-amp-evaluation tool. The program does a simple evaluation using National Instruments' LabView engine. Once you select a part, the tool switches to using National Instruments' MultiSIM full-SPICE engine if a part model is available. In addition to the SPICE tools, Analog Devices, National Semiconductor, and TI also offer Web tools to help design instrumentation amps or to properly bias a single-ended amplifier, as well as for scores of other applications.

For designing filter chains, TI offers its FilterPro software. This downloadable software performs the math calculations to show you the response of multipole filters. National Semiconductor offers its Webench online environment for designing filters. It runs SPICE simulations online to show you the response of the part.

Selecting op amps can be daunting. In addition to conventional voltage-feedback amplifiers, many specialty amplifiers exist (see **sidebar** "Specialty op amps," pg 48). You may need to read relevant trade magazines and books before you understand all the subtleties of amplifier selection. Application engineers can be a great help in getting you to understand the right specifications and amplifier types at which you should be looking. Once you know those facts, you can use the variety of downloadable selector guides and online guides. You can then simulate your circuit online or through the downloadable tools, as well as use the vendor-supplied SPICE models to simulate you circuit in Orcad, Altium, PADS, or Electronics Workbench. EDN

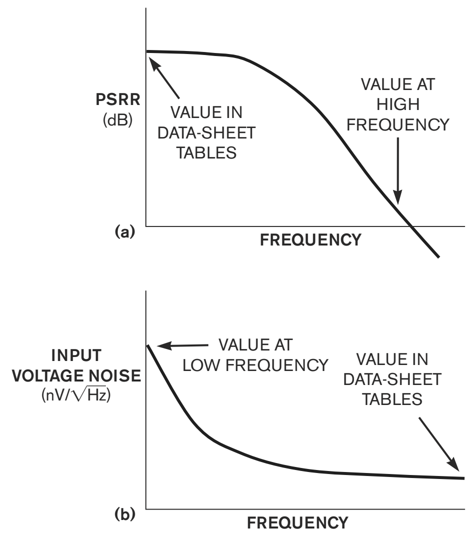

Figure 3 Data-sheet tables often overstate performance. The data-sheet tables list PSRR at dc, at which it is rarely an issue. The data-sheet chart shows where PSRR falls off drastically at high frequencies (a). Similarly, the tables list the input-voltage noise at higher frequencies where the noise is in the flat band (b).

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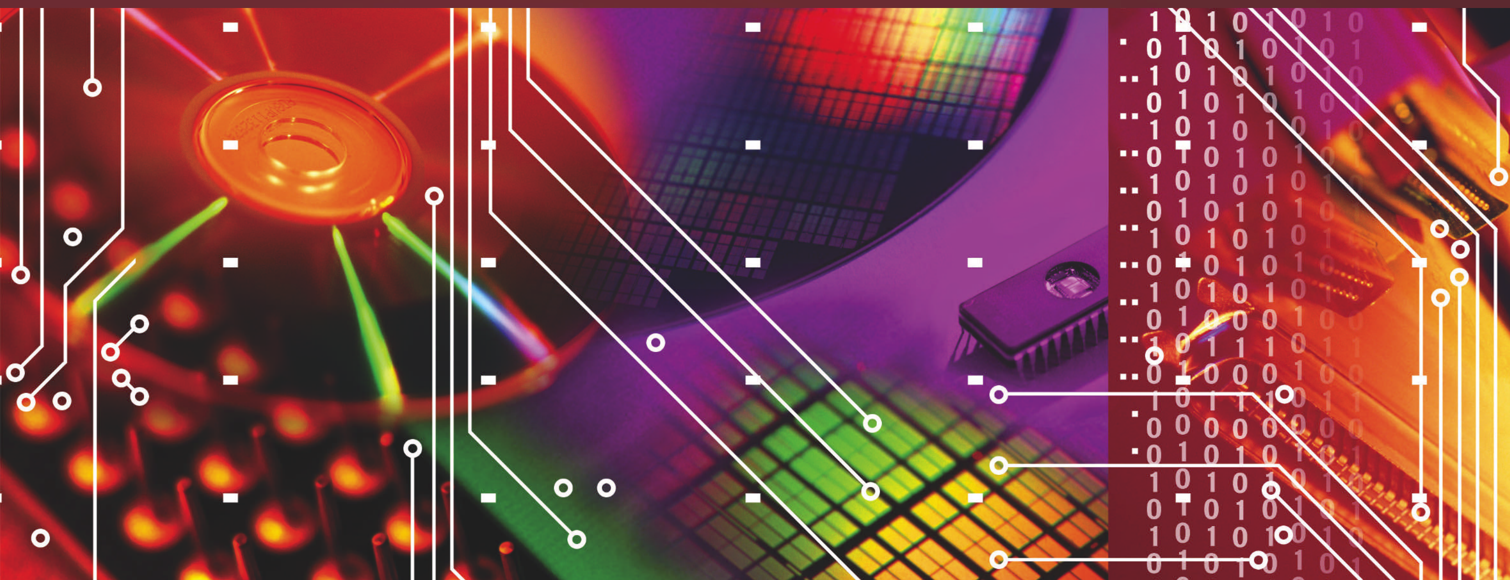

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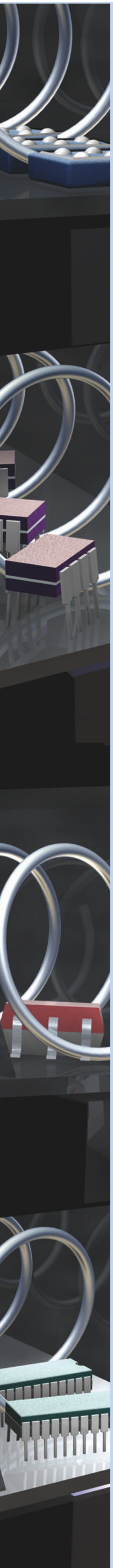

SPECIALTY OP AMPS

Designers often predicate their selection criteria for operational amplifiers on the use of a mainstream amplifier. Several specialty types of amplifiers are available. The most common are current-feedback amplifiers, which find use in video and DSL (digital-subscriber-line) applications requiring high slew rates (Figure A). Another unique benefit is that higher gains do not reduce the bandwidth. An amplifier that can provide the same gain to the higher bandwidth components of a signal has less distortion than one that does not. Current-feedback amps thus suit use in applications requiring high speed and low distortion.

Another specialty amp, the compound amplifier, may use discrete transistors or have multiple amplifier stages inside–that is, several amps for one signal rather than multiple-part packages. For example, the Cirrus Logic CS3001 family has an open-loop gain of 1 trillion, or 300 dB–a sure sign that more than one amplifier is in the signal chain. The phase response indicates that this part is a compound amplifier, suitable for instrumentation. Huge gain means low distortion.

Another form of compound amplifier is the chopper, or autonulling, amplifier. These amps, also called autozero amplifiers, have a second amplifier that is constantly correcting the offset voltage. This feature suits the parts for dc-instrumentation uses, especially because the offset correction also removes low-frequency noise. The disadvantages are that these parts are slow, and their chopping frequency, typically in the 100- to 35,000-Hz range, bleeds into the outputs. This frequency is far beyond the intended frequency of interest, and subsequent circuit stages filter it out. One notable exception is National Semiconductor's LMP2011, which has the microvolt offsets associated with chopper amps yet also has a 3-MHz bandwidth. This device also provides better transient response and slew rates than other chopper amps.

Differential-output amplifiers provide an audio-signal path that is immune to ground loops or to buffering differential-input ADCs. Differential-output audio amplifiers operate in the kilohertz range, and ADC buffers operate in the gigahertz range.

Instrumentation amplifiers are often compound amplifiers with three amplifiers to allow the inputs to work over a large common-mode range. When you change the voltage on the plus pin of a conventional amplifier, the output voltage tracks that input voltage, with the difference between the input pins providing output beyond that level. Instrumentation amplifiers, on the other hand, have reference pins that set the output reference to the desired voltage, which is usually ground. This feature makes them useful for measuring Wheatstone-bridge sensors, such as strain gauges, and for measuring high-side currents. The downsides are reduced speed and high cost. Instrumentation amps often target use for dc signals. Some, such as the PGA206 from Texas Instruments' Burr-Brown division, have bandwidths of 5 to 0.5 MHz, depending on gain. The parts have digitally programmable gain and use JFET (junction-field-effect-transistor)-input stages to provide low noise and high speed.

Other specialty amplifiers have fallen out of favor but are still useful to the analog gurus that know how to use them. Transimpedance amplifiers, such as National Semiconductor's LM13700, have variable gain. They multiply an input current on a control pin by the voltage across the amplifier inputs. The data sheet is worth reading just for the plethora of applications it covers (Reference A). The company's LM3900 Norton amp is obsolete, but its LM359 is still in production. The amplifiers employ Norton's current laws, which work on a current difference into current mirrors as opposed to the voltage-operated input-differential pair that almost all other amplifiers employ. The parts are fairly rare but can provide an interesting exercise in analysis and understanding (Reference B). On Semiconductor's MC33304 power-adaptable amplifier is also obsolete but is interesting because its quiescent current and frequency response would increase whenever the output sourced more current than a user-selectable threshold.

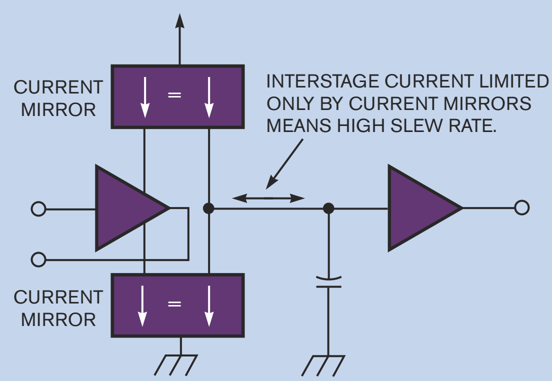

Figure A Current-feedback amplifiers find use in applications requiring high slew rates. The "tail" current of an input-differential pair does not limit the slew rate.

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A "LM13700–Dual Operational Transconductance Amplifier with Linearizing Diodes and Buffers," National Semiconductor, 2007, www.national.com/mpf/LM/LM13700.html.

B "LM359 Dual, High Speed, Programmable, Current Mode (Norton) Amplifiers," National Semiconductor, August 2000, www.national.com/ds/LM/LM359.pdf.

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Make front-end power predictable

ACHIEVING A PREDICTABLE POWER-CLOSURE FLOW MEANS MAKING POWER A METRIC AND A CORE PART OF THE PROCESS FROM THE EARLY STAGES OF DESIGN CONCEPTION.

Power closure has moved to the forefront of design challenges for today's chip projects. Leakage power increases with each new process generation. Smaller geometries enable designs to fit more functions into less space, running at a higher speed. This situation creates exponential growth in power density, presenting a heat-removal challenge for all types of design, especially high-speed applications whose power you've never had to worry about before.

As if meeting aggressive frequencies and managing power consumption were not big enough challenges on their own, frequency and power are actually opposing forces. In other words, optimizing for speed causes an increase in power, and, conversely, techniques to reduce power reduce speed.

This effect most often manifests itself during physical implementation, when long wires make timing closure more challenging. At this point, timing optimization generally involves upsizing; using low-voltage-threshold, high-leakage-power cells; buffer insertion; and other techniques that increase power. It is generally too late in the design cycle to make changes to the RTL structure or the power architecture or to use techniques such as multiple-supply voltage or power shut-off. Such modifications would require you to repeat functional verification, not to mention another spin through implementation. As a result, logic designers feel helpless, left to hope that power consumption won't require a different package, the removal of functions, or other drastic measures that would cause the project to miss its market window. **Figure 1** illustrates a typical power-unpredictability scenario. As tapeout nears, the designer must decide whether to sacrifice costs and, for example, add an expensive cooling mechanism or sacrifice the schedule to rebuild.

The root cause of the problem is that few designers effectively enough measure power in the process when they can take action. The logic designer's lament is "If I had only known earlier, I could have done something about it." What can you do to improve power predictability?

To solve the power-predictability problem, you first need to outline how design decisions affect power in the design flow and what you can do to measure and influence these effects. It is also important to highlight that, as with other design problems, decisions and actions you take earlier more broadly affect the outcome. The flip side is that predictions you make earlier are less accurate. So, try to experiment early with broader, coarse-grained techniques, and, as you begin to solidify the implementation, you'll have more accurate predictions and be able to employ finer grained techniques.

The first factors that affect the power consumption of the chip are the chip specifications: Think about what functions the chip will contain; having more functions means adding more power. Determine the necessary frequency, either for the chip or for the major blocks; using higher frequency means having more power. Consider what process geometry this design will use; using smaller geometries means having higher leakage power and more heat density. Although business or market factors generally drive these decisions, power consumption affects chip sales.

The next two factors affecting power consumption impact each other, so some amount of concurrency and iteration exists between them. The first is operating profile—that is, what will the chip do? If the chip is for a simple cell phone, it will probably spend an hour or two a day in use as a phone; the rest of the time, it will be somewhat idle. A networking chip might have certain ports active much of the time and others active

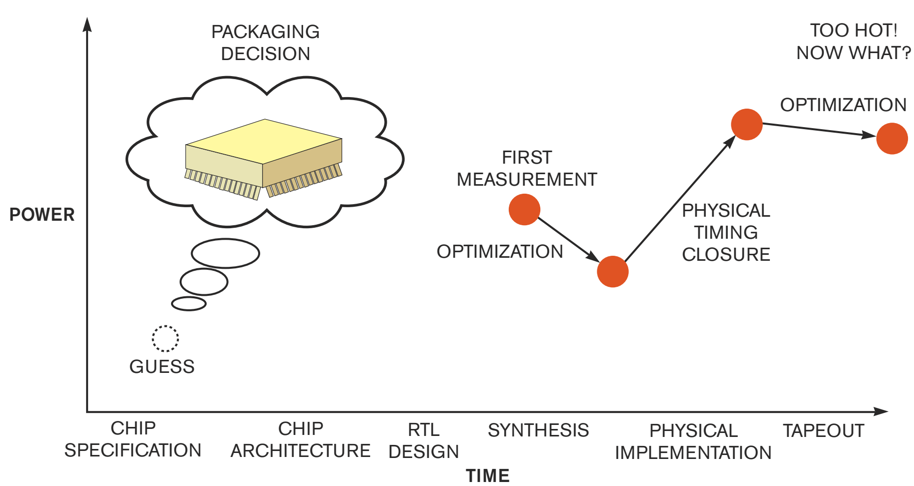


Figure 1 Few designers effectively enough measure power early in the process when they can take action.

only when handling peak loads. If it is a multimedia chip, the operating profile will drastically affect which parts of the chip are active and when. As you might expect, the operating profile will drive the implementation architecture, which is the next factor to consider. In other words, can the device shut off power to certain blocks when they are inactive? Can it run some blocks at lower speeds to lower the operating voltage? Alternatively, can it run them at high speed only sometimes? If so, you can dynamically lower the voltage and, thus, the frequency. The implementation architecture in turn has a small effect on the operating profile, as you add extra power-management functions to the chip, the software, or both.

Once you decide on the implementation architecture, you can begin implementation. In the logical world, this step means synthesis and test-structure insertion. At this stage, you can do more to reduce power, albeit at a smaller order of magnitude than at the architectural stage. Clock gating and the use of multivoltage threshold libraries are two popular techniques during synthesis. Modern synthesis tools also create logic structures to minimize power. And modern test-insertion tools now optimize for power reduction on the tester through insertion of control logic to shut down power domains or even through the use of reduced pin testing. All of these factors affect chip power consumption, and you must account for all of them when trying to obtain early insight into what power consumption will be. Finally, physical implementation involves trying to meet the frequency targets in the face of long wires, huge clock trees, and signal-integrity effects without causing power consumption to grow out of control.

WHAT CAN YOU DO?

Now that you understand where the design sees power effects, you can take steps to improve predictability. The first step in improving the predictability of any process involves establishing measurement criteria. In other words, you need to create metrics and tasks toward which you can track progress and take immediate action when necessary. Fortunately, chip designs all start with a detailed specification that you can capture to establish these metrics and milestones. Monitor progress regularly throughout the project so that you can correct the course quickly if problems arise. The goal is to avoid surprises late in the project, when it is too late to make necessary changes.

As mentioned, although business and the market drive the design specification, the spec has its largest impact on power. Thus, it is important to make specification decisions with as much insight into power effects as is possible. You typically achieve this goal by looking at what others have done before and applying a "process-shrinkage factor" to it. However, with so many variables affecting power consumption at such a large magnitude, this method is too rough to accurately guide this decision. You instead need a method that combines the experience from previous designs with as much real implementation information as possible—an approach that you can carry out by combining early physical prototyping with RTL-power estimation. You can retarget the parts of the design that you reuse in the new context using the new libraries, which enables a more accurate estimate that reflects implementation-specific details. You can still estimate the remaining measurements, but, instead of using them as just numbers in a spreadsheet, you can represent these estimates as design objects. This method provides an early chip-level prototype that can drive future decisions, and you can refine it as more details become available during design.

Of course, a big part of estimating power consumption is the operating profile, or switching activity, of the design. The early prototypes can use estimation you base on default switching activities, because the measurements are rough, and because not all the RTL is available to generate switching activity. However, implementation requires more detailed input, so actual switching activity is necessary. It is important to ensure that switching activity accurately represents the projected operating profile of the chip. Functional-verification testbenches are insufficient for this task. They focus on as efficiently as possible covering all functional scenarios—in other words, without much repetition. Going back to the cell-phone or networking-switch example, real operating profiles involve much repetition and rarely spend time in the corner cases that are the focus of verification. Thus, the best method for capturing switching activity is to have separate simulation runs to capture operating activity. Because this approach can often take a long time, hardware acceleration can greatly improve efficiency. Emulation is the ideal method, because it runs the actual software and can generate a good sample size of switching activity.

Accurate switching activity requires most of the RTL to be complete, so designers often do it concurrently, or iterating, with specification of the power-implementation architecture. At this step, you make implementation trade-offs—that is, you determine which parts of the chip are performance-critical. Doing so dictates the appropriate voltage levels to use or whether you should employ a variable technique, such as dynamic voltage and frequency scaling. It also looks at which

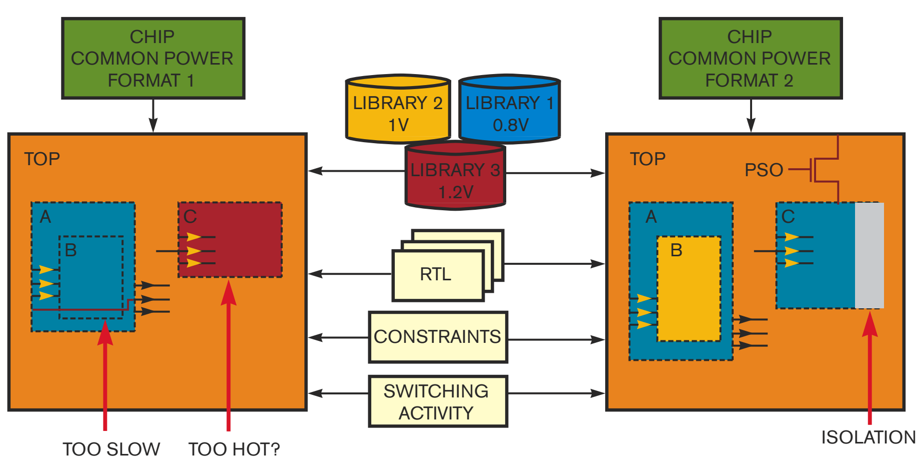
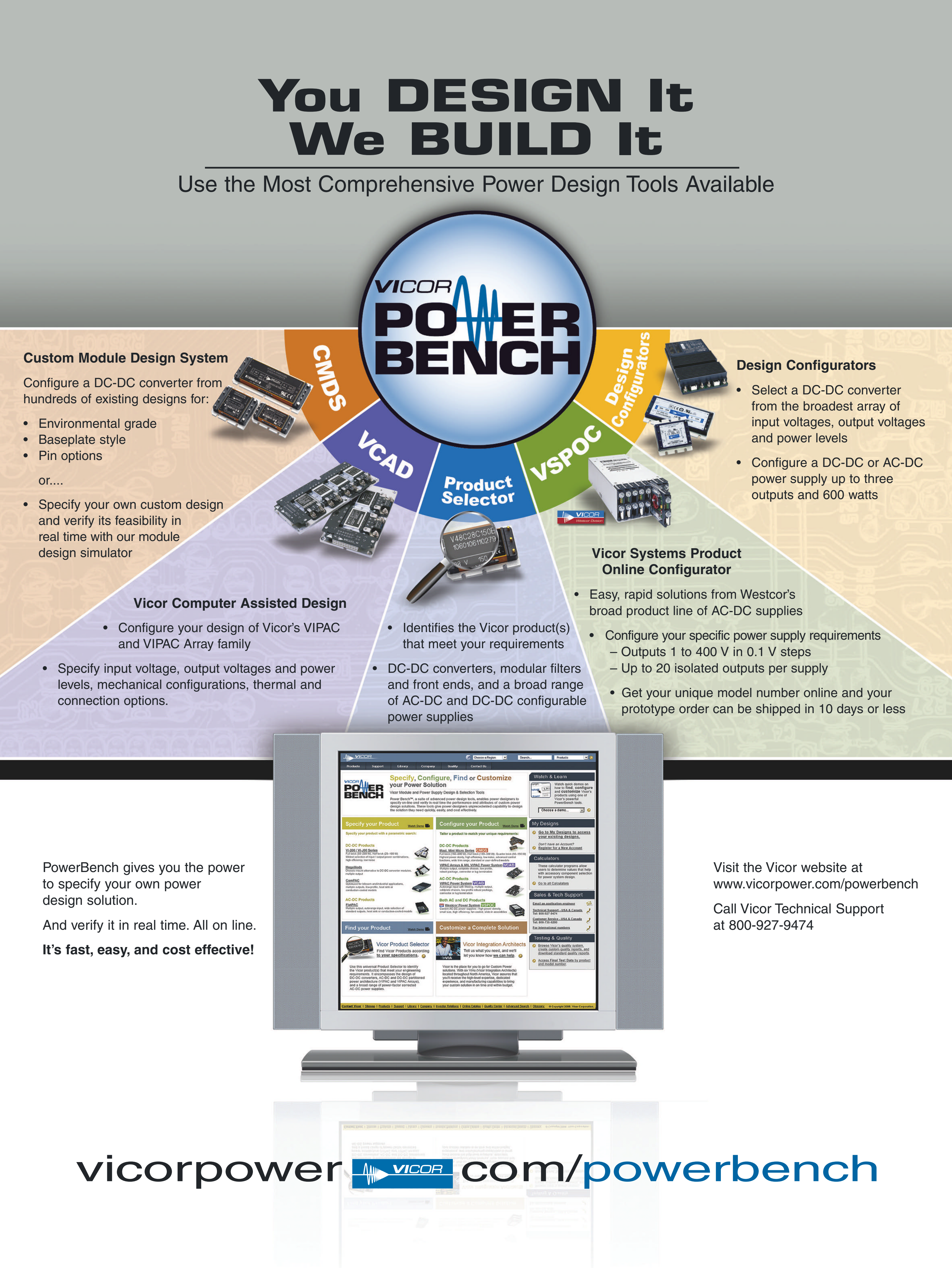


Figure 2 A what-if power-architecture exploration uses a common-power-format specification.



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parts of the chip have long periods of inactivity and therefore are suitable for shutting down to conserve leakage power. If you shut down a block, how quickly does it need to power back up? A full reset cycle is often too slow. Dumping to an always-on memory is one way to speed recovery. The fastest way is to use state-retention registers, which are master-slave flip-flops with the slave flip-flop connected to an always-on retention power rail. As you might expect, this approach incurs an area penalty and requires extra power routing, so use it judiciously.

The implementation architecture has a large effect on power, but you must also balance power goals with frequency goals and implementation feasibility. Therefore, spend time performing what-if analyses to predict the power-timing-area-complexity trade-offs. You can quickly complete this task with RTL-power estimation. But, as the choices narrow, use a more implementation-accurate measurement—either actual synthesis results or, ideally, a silicon virtual prototype. Remember the functional impact of this approach: The architecture impacts system and software design, as well as functional verification. It is therefore important to address this issue as early and as holistically as possible. The most efficient way is with a central specification of the power-implementation architecture that allows a single change to propagate across the flow. At the end of this exercise, you will have a good idea of the power consumption, timing feasibility, physical feasibility, and functional correctness. **Figure 2** depicts what-if power-architecture exploration using a common-power-format specification. From this point, you can move toward more detailed implementation and finer grained analysis and optimization.

Synthesis is often the point at which design teams start to predict and track power consumption. It is late to start at this stage, because this step has a smaller effect on overall power consumption than architecture, but it is an important step in creating a design that closes during physical implementation. So, it is still important to predict power consumption at this stage. You can use timing-aware RTL-power estimation to start to see relative block power consumption that will result from synthesis. If any block uses more power than you'd expect, you can address that problem early through rebudgeting, fixing RTL, fixing constraints, and other methods. You should also run gate-level power analysis along with timing analysis after every synthesis run that the system performs during RTL design. It is always easier to make changes earlier than later, so measure power whenever you look at timing.

At this stage, you insert clock gating, so any predictions must be aware of what the clock-gating engine will do—that is, whether it will do multistage clock gating and whether it will use enable logic from a different hierarchy from the registers. The predictions must also be aware of the minimum and maximum register constraints and other factors. Also, the logic structures that the system creates during synthesis have a great effect on

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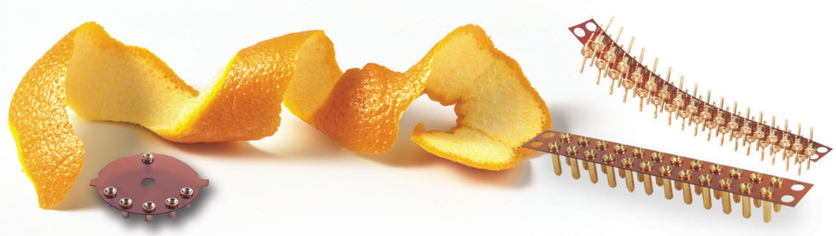

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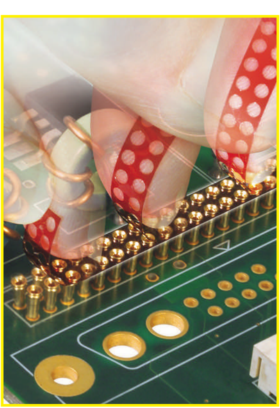

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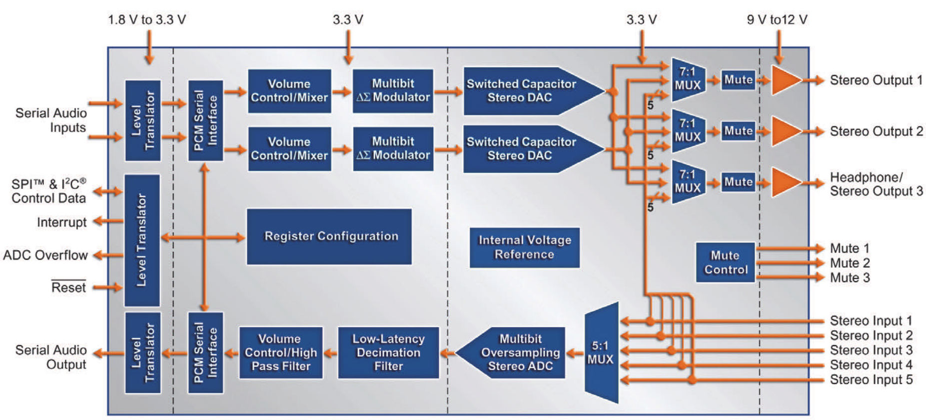

CS42325

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Part	Resolution	Dynamic Range	THD+N	Sample Rate	Analog I/O	Power Supply	Comments	Package
CS42324	24 bits	100 dB D/A Converters 95 dB A/D Converters	–90 dB D/A Converters –88 dB A/D Converters	96 kHz	10 Single-ended inputs 6 Single-ended outputs	VA = 9 V or 12 V; VD = 3.3 V; VL = 1.8 V or 3.3 V	4 DAC, 2 ADC 2 V_{RMS} I/O, I/O mux	48 LQFP
CS42325	24 bits	100 dB D/A Converters 95 dB A/D Converters	–90 dB D/A Converters –88 dB A/D Converters	96 kHz	10 Single-ended inputs 6 Single-ended outputs	VA = 9 V or 12 V; VD = 3.3 V; VL = 1.8 V or 3.3 V	4 DAC, 2 ADC, Stereo Head-phone Driver 2 V_{RMS} I/O, I/O mux	48 LQFP

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- –90 dB THD+N
- Integrated line driver
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  - 3x stereo single-ended outputs
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- Volume control with soft ramp
  - 0.5 dB step size
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- Selectable serial audio Interface formats
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- Popguard® technology

A/D Features

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- –88 dB THD+N
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power. A structure that is too slow will require upsizing, or "down-thresholding," during physical design, causing a power increase. Any structure that is too fast consumes more power than necessary. So, optimization that focuses on simultaneously satisfying multiple objectives is key to creating a netlist that incorporates more predictability into the physical design. Finally, using a more physically realistic model of wire timing is essential in creating structures that will meet frequency targets without being overpowered.

The logic-design team sees physical implementation as a process over which it has little control yet during which power surprises happen. However, many of the above steps can prevent these surprises. If a multiobjective synthesis engine creates a well-balanced logic structure, the engine will much more cleanly close in on your timing goals in physical implementation, requiring less powering up. And, if the system performed and refined silicon prototyping as it checked in blocks, you should have a good idea of how physical implementation will go. You can refine the early silicon virtual prototype that the system used during specification as the system synthesizes blocks, constantly reflecting the metrics you specified up-front. This method enables earlier fixes to problems so that they do not cascade forward and ultimately require late changes that necessitate reverification. Front-end teams are not yet widely using silicon virtual prototyping because of the use model; however, the method can have tremendous benefits. Some synthesis tools now offer the ability to run silicon virtual prototyping right from the synthesis cockpit, where you can perform synthesis analysis and reoptimization. This ability arms logic-design teams with the ultimate in predictability for timing, area, and power.

Achieving a predictable power-closure flow goes beyond just doing early estimation. It requires power to be a metric and a core part of the design from the early stages of conception that you must analyze and re-evaluate throughout the process. It requires some changes to design methodologies, to take advantage of modern power-reduction techniques. And it requires some changes to EDA tools to enable fast timing-power-area trade-offs and to generate globally balanced logic structures that do not blow up during physical implementation. Power has begun to profoundly impact the market and technical feasibility of digital ICs. It seems only logical that the way to address it is through a holistic approach to managing power predictability. EDN

AUTHOR'S BIOGRAPHY

Jack Erickson is a product-marketing director at Cadence Design Systems, where he is responsible for the Encounter RTL Compiler synthesis and Cadence Logic Design Team Solutions. He has been with Cadence for 14 years and holds a master's degree in business administration from Worcester Polytechnic Institute (Worcester, MA) and a bachelor's degree in electrical engineering from Tufts University (Medford, MA).

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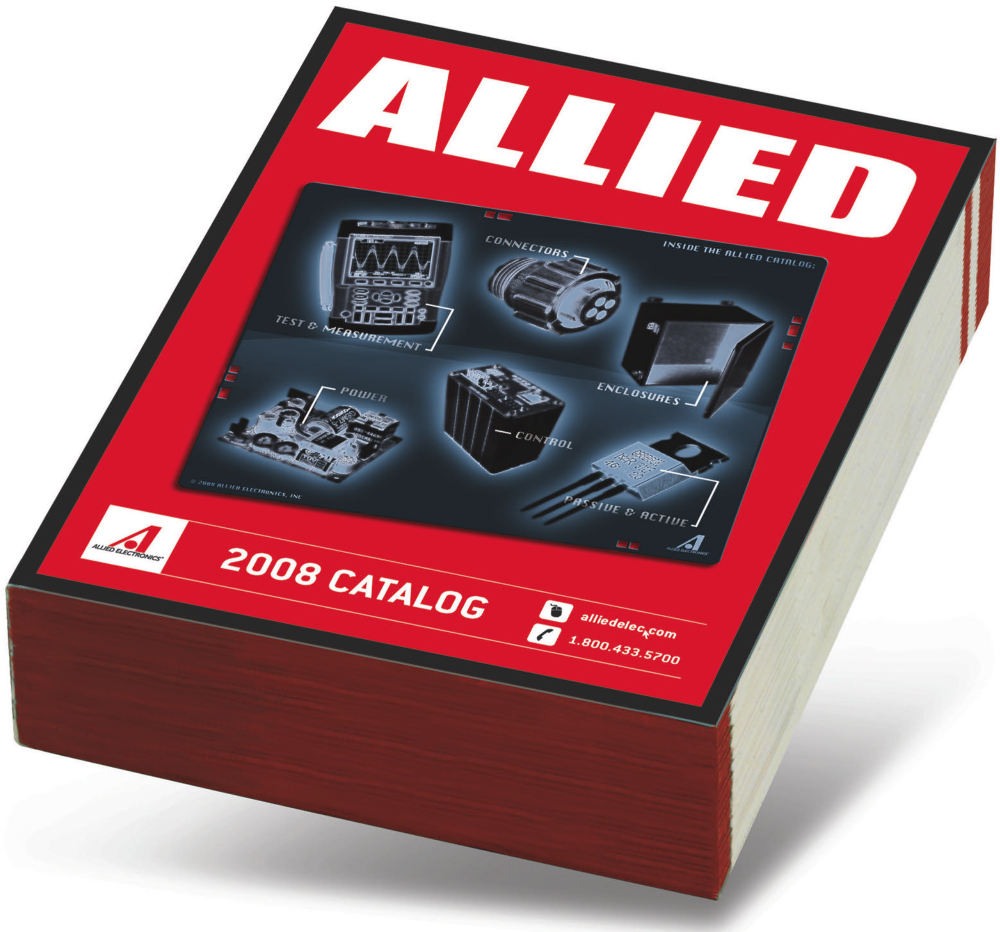

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BY TERRY CLEVELAND • MICROCHIP TECHNOLOGY

Digitally managed power circuits

MANY POWER CIRCUITS NEED DIGITAL CONTROL. THOSE COMBINING DIGITAL- AND ANALOG-CIRCUIT BLOCKS PROVIDE THE BEST OF BOTH WORLDS.

Power ICs that combine analog and digital are becoming more common. Battery-charger applications have increased the need for digital functions, but high frequency and cost have limited the practicality of closed-loop, purely digital systems. Combining both analog and digital control of the power-conversion feedback loop can help designers achieve the best of both the analog and the digital worlds.

Historically, many power-management designs have been analog-only. However, with the development of small, low-cost microcontrollers, power-system designers are now integrating digital features into their power systems. The following design examples include both digital and analog components and features. Digital features include host communication, output-voltage/current programming, fault diagnostics and management, timers and housekeeping, and others. Analog components and features include MOSFET drivers and current and temperature sensing.

For purely digital systems, you determine the duty-cycle variable by using a computing algorithm. By knowing the previous duty cycle, the rate of change since the last computed variable, and how much it has changed over several switching cycles, you can calculate a new duty cycle. For purely analog PWM (pulse-width-modulated) control systems, you determine the duty cycle using a high-speed comparator. When the inductive ramping current and the dc signal of the error amplifier are equal, the duty cycle terminates. The dc-error signal follows linear-control-system behavior, limiting its speed of response because of the power-supply time constant and the linear-control system's gain.

For applications with basic requirements, such as simple dc/dc-voltage regulators, engineers commonly use analog designs. For very-high-end motor-control applications, on the other hand, digital-control systems offer many advantages over simple analog-control options. For example, you can control motor speed using a variable-duty cycle that the host system communicates. In fact, it may communicate several variables to the digital system, which makes duty-cycle decisions.

Two key considerations in choosing between analog and digital control are size and cost. The power-handling capability, which the systems' passive-filtering components dominate, typically drives the power-system size. In the case of a buck converter, the input capacitors, buck inductor, and output-filtering capacitor determine the size of the option. The converter's switching frequency greatly impacts the size of these components.

In high-frequency converters, digital products are limited in speed and resolution. For example, for a 500-kHz dc/dc converter with a 1.8V, 1% output, a digital-control option would require a PWM-generator frequency of 284.4 MHz. This value is impractical in many applications, especially battery-powered applications in which quiescent current is at a premium. However, very-high-power systems that switch at low frequencies typically require digital features, so digital-control-system designs are more practical. Offline-PFC (power-factor-correction) designs are increasingly full digital-control systems to minimize losses and switching below the bottom of the EMI (electromagnetic-interference) specification, at which the converter-switching frequency is on the order of 125 kHz.

LI-ION-BATTERY CHARGER

The first application is a bidirectional dc/dc converter for multiple Li-ion (lithium-ion) batteries in series. This application requires a complete charge profile for four series-connected Li-ion cells, charged at a 2A fast charge from a 7V input. Charging Li-ion batteries involves several stages. The first stage is to measure the pack voltage to determine whether it is within an acceptable range. Fast charge currents can damage a deeply discharged battery pack. If the pack voltage is in an acceptable range, the converter can initiate a charge cycle that comprises a precharge (low constant current), a fast charge (high constant current), and a constant-voltage phase

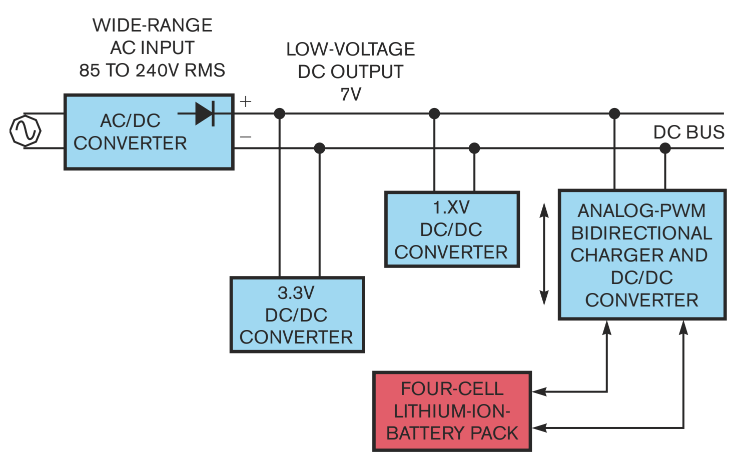

Figure 1 This application uses a mixed-signal-design approach to control the bidirectional power train.

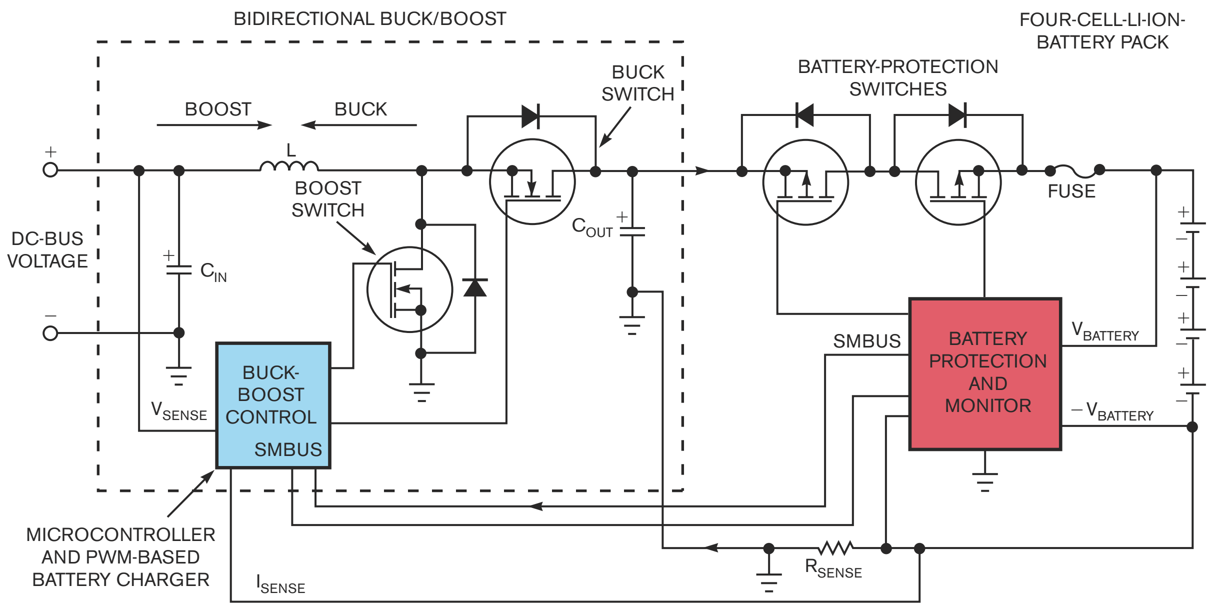

Figure 2 A synchronous buck-boost converter using two N-channel switches develops the bidirectional capability.

and proper-charge termination, which you base on a percentage of rated pack capacity. During this charge phase, you can measure the pack voltage using an ADC or digitally, using the microcontroller's communication capabilities if the design employs a "smart" battery pack.

If the design is without the 7V input source, the Li-ion-battery pack can provide a regulated voltage to the system. In this application, the 12 to 16.8V battery-pack voltage is stepped down to 6V and can deliver 15A, approximately 90W of power. If you suddenly remove the ac-derived input, the voltage on the 7V input must not drop too far, or the system processor will reset.

While charging the battery, the step-up, or boost, converter is a current source. As with all current-source applications, output-overvoltage protection is necessary to protect the power system from damage when you remove the load or batteries.

High switching frequency and high efficiency are key for this battery-powered application. The compromise between switching frequency and size happens at 500 kHz.

This application uses a mixed-signal-design approach to control the bidirectional power train (**Figure 1**). The dc-bus voltage is typically 7V when the ac/dc converter is present. This 7V source powers the system and charges the four-series-cell Li-ion-battery pack. If you remove the 7V source, the system control stops the charging process and starts the dc/dc-step-down-converter process to regulate the dc-bus voltage to 6V. Additional dc/dc-converter loads attach to the dc-bus voltage. A synchronous buck-boost converter using two N-channel switches develops the bidirectional capability (**Figure 2**).

In this application, the microcontroller runs the battery-charge algorithm. By sensing the dc-bus voltage to determine whether the 7V input is present and sensing the battery-pack voltage to determine its charge state, the microcontroller initiates a charge cycle. The bidirectional power train is a programmable current source when charging the battery and is a voltage-regulated dc source when you remove the 7V input. The system achieves this flexibility by summing two analog-control loops to develop the charge algorithm. The microcontroller programs the proper current, and the constant-voltage phase of the charge cycle uses its ADC to sense pack voltage. When the pack voltage increases to 16.8V, the GPIO (general-purpose-input/output) current reference decreases by 1 bit, lowering the charge current. When the charge current reaches 7% of the pack capacity, the charge cycle is complete. Safety timers prevent the charger from continuously charging into a faulted pack, and the system regulates the buck voltage to 6V using a simple resistor divider. **Figure 3** shows a mixed-signal control loop.

When the 7V-dc bus is present, the voltage-amplifier (V_{AMP}) inverting input is above the 2.5V reference-voltage noninverting input, and the amplifier output is pinned at ground. This situation provides a "virtual" ground for the current-amp output divider. When you remove the 7V-dc bus, the amplifier-current noninverting input is negative, as current reverses in the battery pack during discharge. The inverting input, which the microcontroller-firmware reference generator sets, is always a positive value, which forces the output of the current amplifier low, providing a virtual ground for the voltage amplifier to work into while regulating the dc bus to 6V.

One challenge with this design is providing the uninterruptible dc-bus voltage over the whole range of Li-ion-battery-pack charge algorithms. The worst case for this situation

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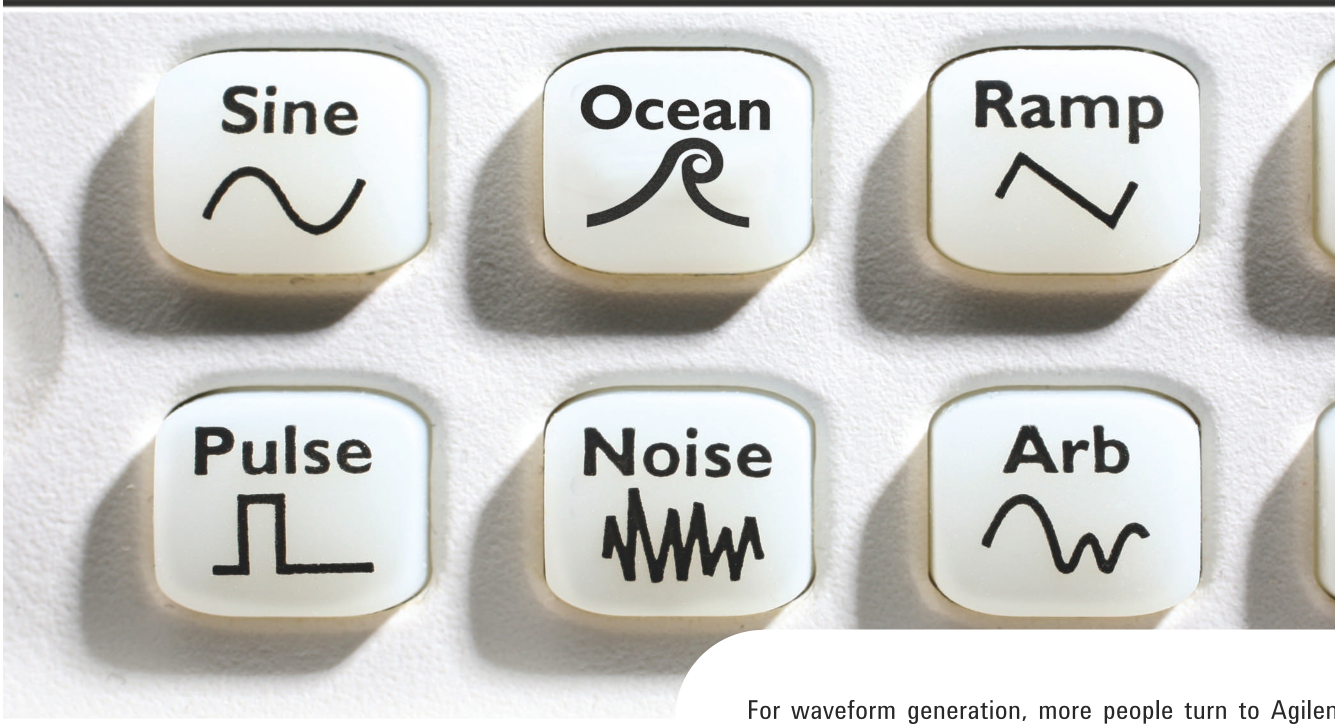

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occurs when charging the pack at maximum current. For this condition, the inductor current must reverse from 2A into the battery and then supply the load current to the dc bus. The handoff of one analog loop to another determines the speed of this dynamic transition.

Another point to consider is that, when the battery pack is fully charged, the synchronous converter must be operating so that it can prevent the dc bus from dropping out. However, in this case, the battery current should be 0A—neither charging nor discharging. You can achieve this goal by using a 10-bit software PWM reference that provides enough steps to be able to set the current close to 0A. However, error terms and offsets can result in a large error because of the use of a small-sense resistor. You can resolve this situation by calibrating the "idle" current in the battery. By measuring the current while sweeping the 10-bit PWM-firmware reference, you can determine the idle-current setting and store it in memory. Therefore, when the battery-pack charge is complete, the firmware-PWM reference sets to the idle state, always ready for the removal of the 7V-dc-bus input.

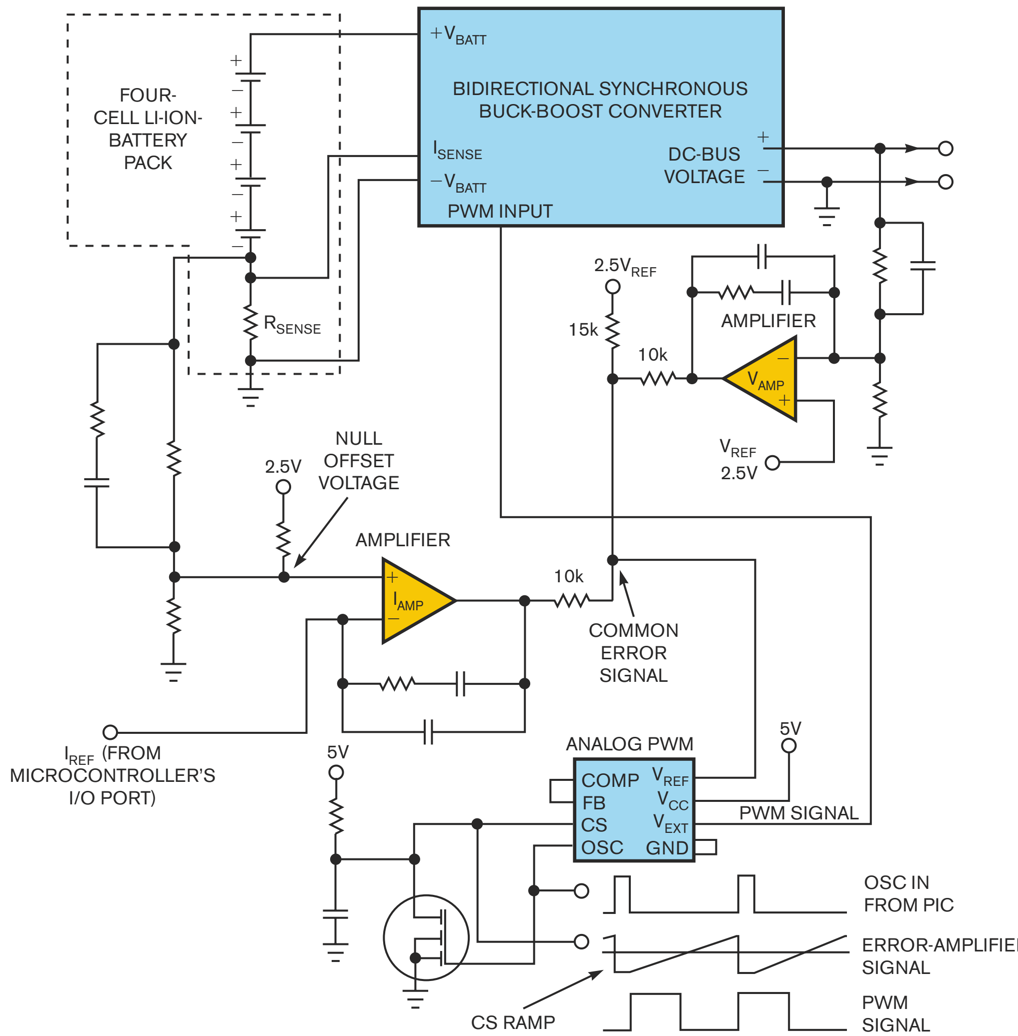

Figure 3 The analog PWM module controls bidirectional energy flow into and out of the Li-ion-battery pack. The reference-current signal from the microcontroller sets the proper charge-current level, using a firmware-generated, 10-bit, PWM reference.

POL CONVERTER

In today's high-end-computing applications, several low-voltage, high-current supply rails are necessary to power the system processors and high-speed devices for video processing. Issues in developing these multiple-rail systems are synchronized switching and frequency dithering to minimize input-ripple currents. Additionally, multiple-rail systems may be necessary to sequence outputs, as well as enable multiple phases to reduce ripple voltage and ease surface-mount manufacturing. Multiple-rail systems also allow an optimal number of phases for tracking load demand, margining the output for system-level testing, and performing housekeeping functions, including undervoltage lockout, power-good signals, reset timing, and overvoltage protection. Because real estate is at a premium for these high-end applications, switching frequency is critical.

Some required parameters for this POL (point-of-load)-converter application include a 12V nominal input voltage, stepping down the output to two 3.3V, 20A outputs, and a synchronous-buck topology for high efficiency. The application also requires a programmable output voltage with voltage-margining capability; full cycle-by-cycle current limiting; a 20A-per-output capability, switching at 500 kHz, 180° out of phase; and independent overtemperature protection on each output-voltage rail. Other requirements include outputs that you can sequence or track during power-up, and programmable input-undervoltage and -overvoltage lockout with programmable hysteresis to prevent the converter from operating under abnormal input-voltage ranges.

This application employs a microcontroller with an ECC (enhanced-capture-and-compare) peripheral. You can use this peripheral to develop two 180°, out-of-phase clocks—one for each PWM input. An important analog-PWM feature is pro-

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BRIEF

New Zero-Drift Amplifier has an I_Q of 17 µA

By Thomas Kugelstadt
Senior Applications Engineer, Industrial Systems

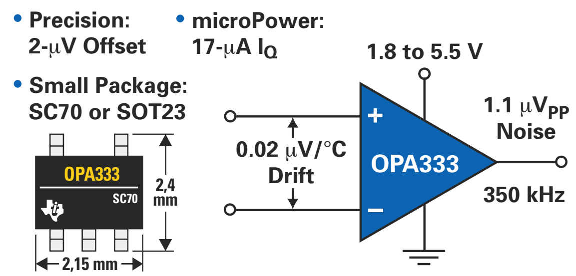

Figure 1. OPA333 performance features

Modern micropower applications require not only a very small offset and offset drift but also very low noise. A front-end, low-noise amplifier combined with signal-conditioning circuitry and an input sensor forms a microsystem that often has to either be portable or stand alone and is therefore battery-powered. Because power consumption has to be small, it is crucial to eliminate the 1/f (flicker) noise and to reduce the overall noise down to the fundamental thermal noise, which is mainly determined by the allowable current consumption of the input stage. A new, micropower, low-noise, chopper-stabilized operational amplifier, OPA333, fulfills these requirements while operating from a 1.8-V supply at a quiescent current of only 17 µA. The amplifier provides a high open-loop gain, A_{OL} = 130 dB, and a 350-kHz gain bandwidth (GBW) at a phase margin of 60°. With typical values for offset and drift of V_{OS} = 2 µV and dV_{OS}/dT = 20 nV/°C, respectively, the OPA333 also generates only 1.1 μV_{pp} of instantaneous noise in the 0.01- to 10-Hz band.

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Also, the voltage-noise spectral density is limited to 55 nV/$\sqrt{Hz}$. The OPA333 offers rail-to-rail input and output and is available in SC70 and SOT23 packaging. Operation is specified from –40°C to 125°C.

Device Description

The OPA333 consists of a high-precision path (g_{m1}, g_{m2}, and g_{m3}) in parallel with a wideband path (g_{m4} and g_{m3}). (See Figure 2.) The precision path ensures a high open-loop gain, while the wideband path provides high gain bandwidth and high phase margin. To achieve high gain while operating from very low supply voltages, the precision path uses a three-stage, nested Miller-compensated (NMC) cascade amplifier. Careful design of the g_m stages and appropriate selection of the Miller compensation capacitances can shift the dominant pole to very low frequencies and the second pole to very high frequencies, which expands the range of stable operation.

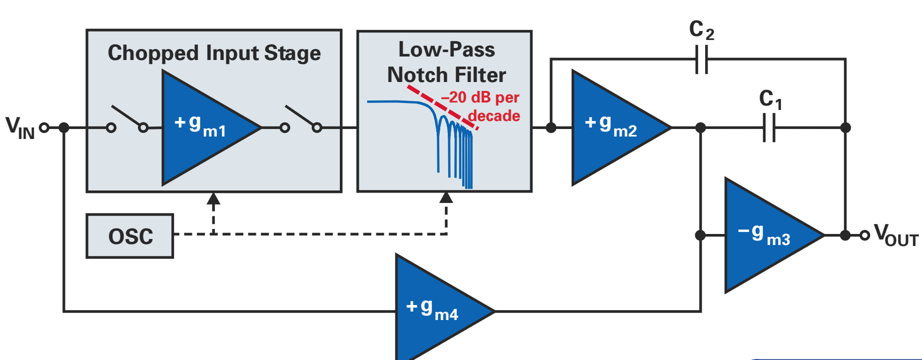

Figure 2. OPA333 simplified block diagram

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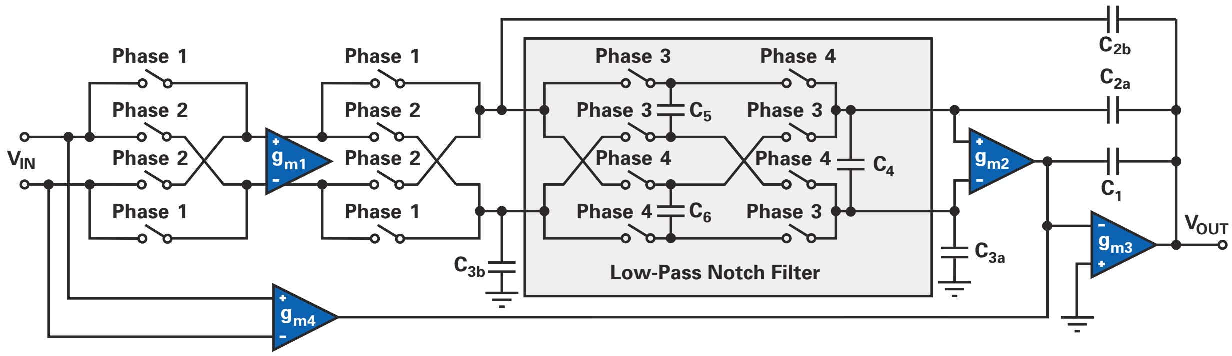

Figure 3a. OPA333 detailed block diagram

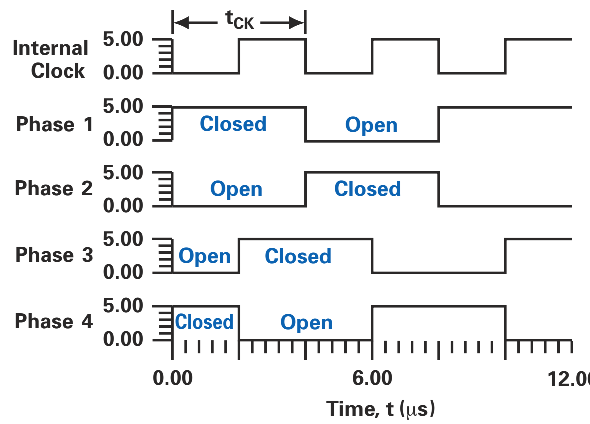

Figure 3b. OPA333 offset-cancellation timing sequence

Offset Cancellation

Figure 2 shows that, except for g_{m1}, the input offset voltages of all other stages are strongly suppressed by the open-loop gains of preceding amplifier stages. Hence the nonattenuated offset of g_{m1} requires active cancellation through either chopping or auto-zeroing.

While an auto-zero amplifier (AZA) removes its offset and 1/f noise at the cost of a raised white-noise level in the baseband, a chopper-stabilized amplifier reduces its baseband noise to the initial white-noise level but generates large output ripple. Because the input-stage noise is inversely proportional to its quiescent current (I_Q), an AZA requires an increase in I_Q to achieve the desired low-noise level. Since this increase counteracts the requirements of a micropower amplifier, it is desirable to use a chopper-stabilized amplifier and find some way to filter the output ripple.

The chopper stage does not introduce wideband folding components into the baseband, but the process of chopping creates increased output ripple because it modulates the offset to a higher frequency range where no noise existed before. To reduce the output ripple by a factor of 500 or more, the OPA333 has a switched-capacitor (SC), low-pass notch filter in the offset cancellation path with filter notches at the chopper frequency and its harmonics.

The Final Amplifier System

Figure 3a shows the actual implementation of the chopper-stabilized amplifier, and Figure 3b shows timing waveforms. During phases 1 and 2, the input signal is modulated. During phases 3 and 4, the capacitors C_5 and C_6 work in tandem. While C_5 is charged with current from g_{m1}, the charge on C_6 is transferred to the integrator, g_{m2}, and vice versa. Note that the input signal is modulated twice, once by the input switches of g_{m1} and a second time by the output switches. Relative to V_{IN}, the polarity or direction of the current from g_{m1} remains the same during phases 1 and 2. However, the offset voltage (or offset current) is modulated only once by the output switches. Its polarity changes from phase 1 to phase 2.

During the first half of phase 3 (that is, $t_{CK}/2$ of the clock period), the phase 1 switches are closed so that the combined signal (I_{SIG}) and offset (I_{OS}) currents from g_{m1} ($I_{SIG} + I_{OS}$) charge C_5. During the second half of phase 3, the phase 2 switches are closed and the direction of the offset current changes so that the charge on C_5 is $I_{SIG} - I_{OS}$. The capacitor's charge is given by $Q = I_C \times t$, with $t = t_{CK}/2$, $I_{C1} = I_{SIG} + I_{OS}$, and $I_{C2} = I_{SIG} - I_{OS}$. Thus, after phase 3 is completed, C_5 has the charge of $Q_{C5} = (I_{SIG} + I_{OS}) \times t_{CK}/2 + (I_{SIG} - I_{OS}) \times t_{CK}/2 = I_{SIG} \times t_{CK}$. The offset-free charge is then transferred to the next stage during phase 4, where the same procedure is applied to C_6.

Summary

The OPA333 is a superior, zero-drift micropower amplifier. Chopper stabilization ensures low baseband noise at very low supply currents. Integrated low-pass filtering removes the output ripple created by the chopper modulation of the input offset. Because an amplifier's noise power density is inversely proportional to its quiescent current, the product ($e_n^2 \times I_Q$) represents a figure of merit, revealing how much additional tail current is necessary to reduce the remaining baseband noise to the desired level after the process of offset cancellation. A more familiar figure is the ratio of gain bandwidth to quiescent current, GBW/I_Q, disclosing how much bandwidth per microampere is achieved. In both figures of merit, the OPA333 demonstrates superior performance versus competing devices.

References

1.OPA333 Datasheet (SBOS351B)
2. ***amplifier.ti.com***

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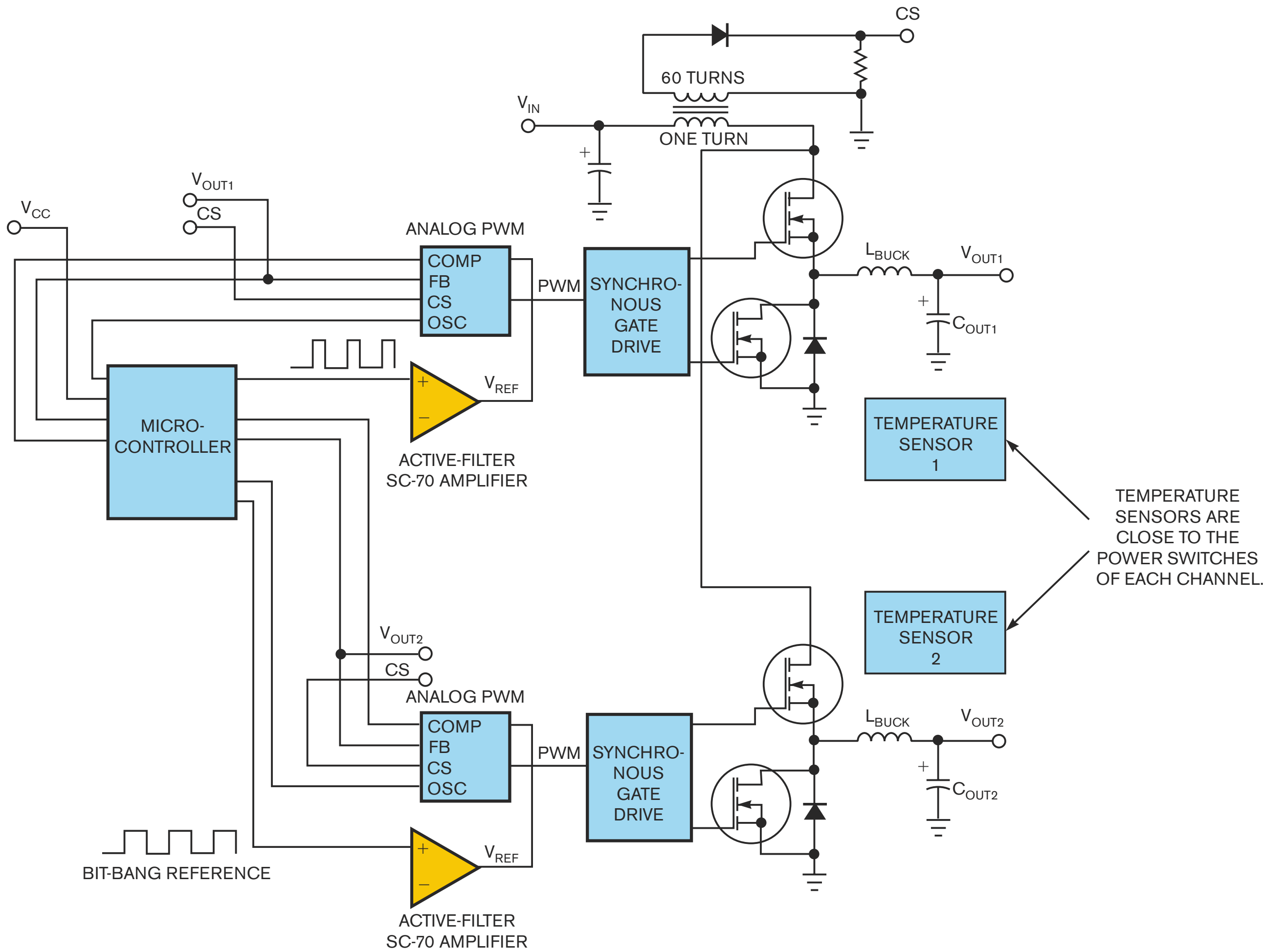

Figure 4 The POL (point-of-load)-converter design combines a microcontroller with two high-speed analog PWMs.

grammable undervoltage lockout with hysteresis. Choosing the proper hysteresis can be challenging, because input impedance is difficult to predict in many applications. With the mixed-signal option, the undervoltage-lockout value and hysteresis develop during system integration without changing hardware. Using the analog PWM to control the PWM duty cycle and cycle-by-cycle current limit reduces the burden on the digital system. By controlling the duty cycle using an analog approach and programming the desired output voltage using a digital method, a high-frequency, programmable power system becomes practical and possible.

The POL-converter design combines a microcontroller with two high-speed analog PWMs (**Figure 4**). The 500-kHz switching frequency reduces the size and cost of the module. The design is capable of 20A output current, with a programmable output voltage of 0.8 to 3.3V from a 12V nominal input.

In this design, the microcontroller generates the two 180°-out-of-phase oscillator inputs, one for each analog PWM. Both offer 50% duty cycle, thus limiting the maximum on-time for each converter to 50%. Limiting the cycle-by-cycle switch current in this application is necessary to protect the power system from external load faults. Additionally, by limiting the maximum duty cycle to 50%, a single current-sense transformer becomes usable for both output voltages (**Figure 5**). The 60-to-1 current-sense transformer provides current-sense information for one phase and then resets and provides current-sense information for the other phase. Two digital-temperature switches offer thermal protection in this design—one for each output-voltage channel. The switches provide independent overtemperature protection. The sensors are mounted near the highest dissipating devices.

The system senses the input voltage using the microcontroller's internal ADC—an action you can compare with preprogrammed values to provide input undervoltage and overvoltage protection. Hysteresis is also programmable in this design, making it easier for the end user to adapt the dual dc/dc converter to varying source-impedance applications. An internal firmware dual-reference generator sets programmable out-

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put voltages. This software digital reference passes through a second-order filter to minimize ripple, because the system represents any ripple voltage on the reference at the output of the converter.

DEVELOP A BOUNDARY

An important decision for both of these application examples is where to partition the analog and digital boundaries. Both applications require some form of digital control. However, full digital control of the power-train duty cycle at a high switching frequency is impractical and fails to meet the necessary size and cost constraints. Therefore, you must develop a dividing line or analog-digital boundary. One method for achieving this goal is to use a simple, high-speed analog-PWM module for this general-purpose boundary crossing.

Another challenge in developing mixed-signal power systems involves protection speed. By using an analog-PWM module that provides 12-nsec performance from current-limit sense to PWM output, designers can overcome this difficulty. Additionally, many microcontrollers have onboard analog functions that assist in protection. In the bidirectional-system application, you can use an internal comparator to sense an output overvoltage condition and disable switching at speeds greater than 200 nsec. **EDN**

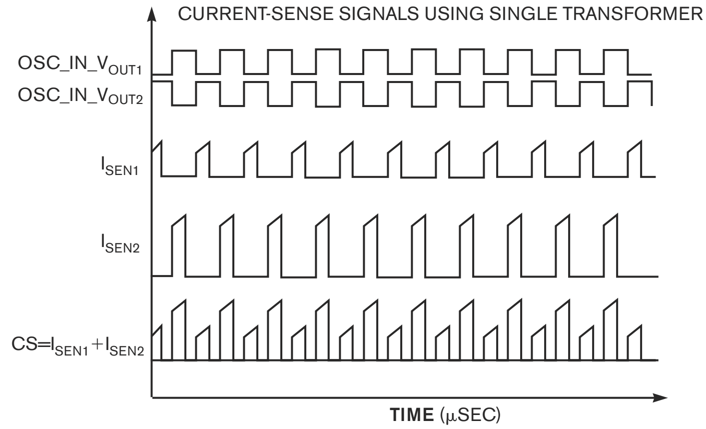

Figure 5 By limiting the maximum duty cycle to 50%, a single current-sense transformer becomes usable for both output voltages.

AUTHOR'S BIOGRAPHY

Terry Cleveland is a staff applications engineer with Microchip Technology's analog- and interface-products division. He has a bachelor's degree in electrical engineering from Polytechnic University of New York (Brooklyn) and a master's degree in electrical engineering from State University of New York (Binghamton, NY).

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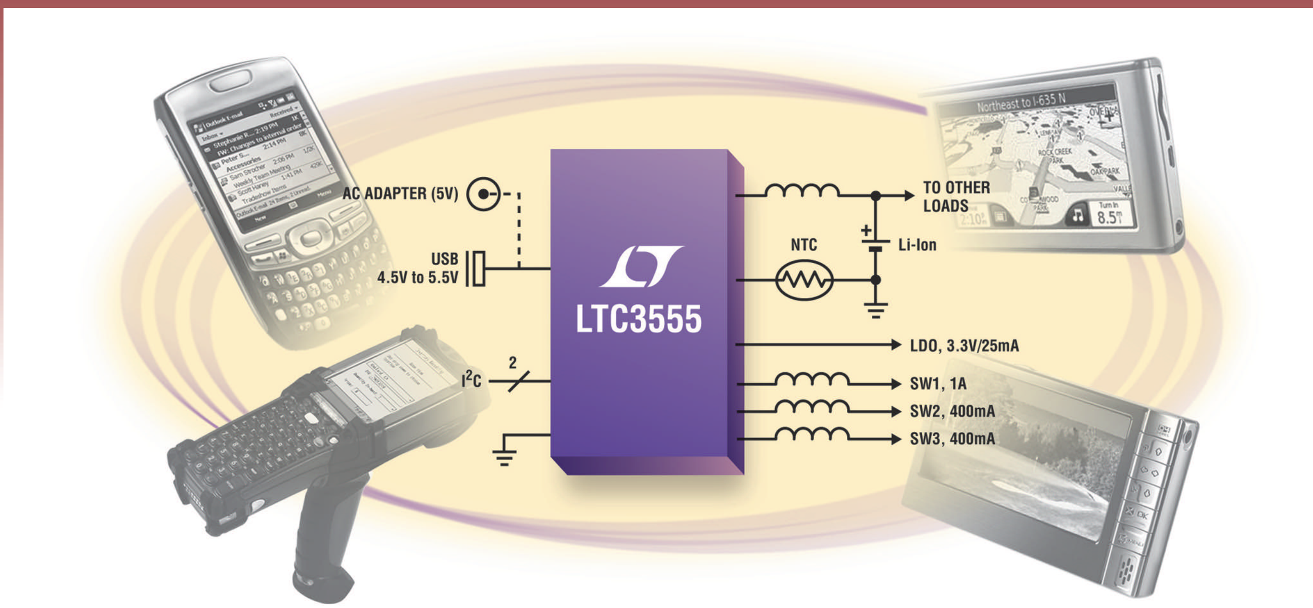

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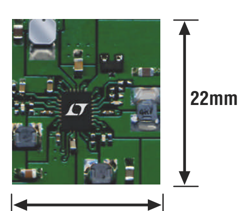

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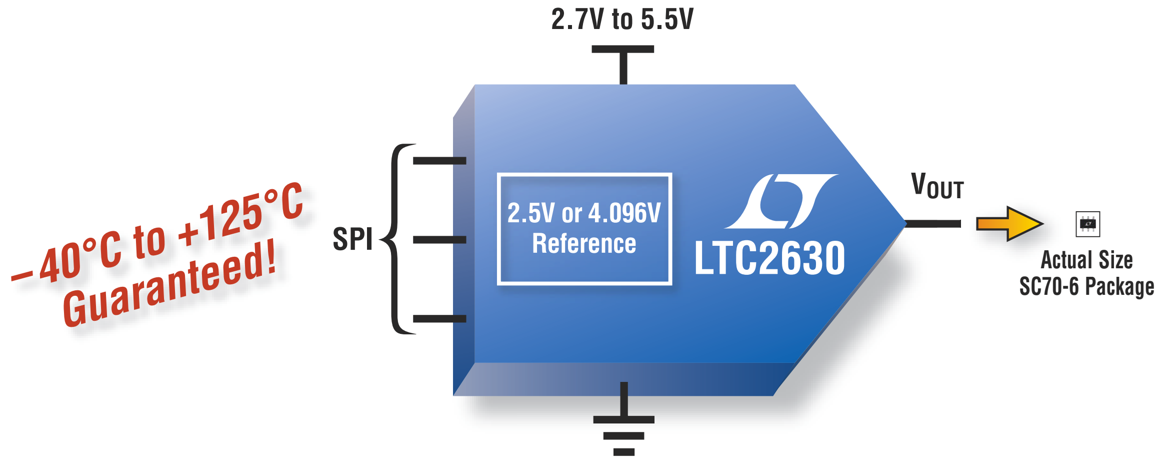

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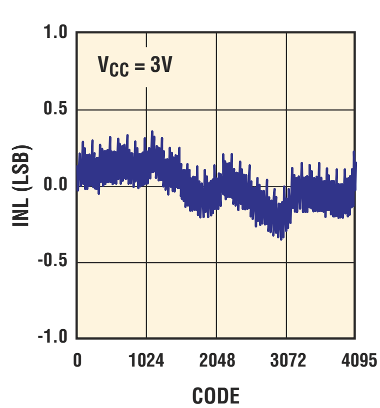

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LINEAR TECHNOLOGY

Use a TL431 shunt regulator to limit high ac input voltage

Todor Arsenov, STMicroelectronics, Prague, Czech Republic

Most isolated, offline SMPSs (switched-mode power supplies), including flyback, forward, and resonant, must operate at input voltages of 90 to 260V rms. Some cases even use line-to-line voltages of 400V rms±10%, leading to increased component-voltage ratings and, thus, increased cost of the overall design. In such cases, it is preferable to use input-limiting circuits, allowing you to increase the input voltage to 440V rms without damaging the power-supply components.

The circuit in **Figure 1** limits, or clamps, input-ac voltages higher than 260V rms to levels safe for the operation of the power MOSFET in an SMPS. The circuit employs MOSFET Q_1 working as a 100-Hz switch and shunt-regulator IC_1, a TL431CZ, setting the clamped high-voltage level by divider R_2 and R_4. The circuit uses the component values shown. The clamped output voltage is 360V dc, the input voltage is 260V rms, and the maximum input voltage is 440V rms. The circuit was tested at power levels of 5 to 10W.

At an input voltage of less than 260V rms, Point C is less than 2.5V, and IC_1 is off, sinking the minimum off-state cathode current. Zener diode D_2 breaks down to 15V, ensuring a stable on-state for Q_1. This operation is the normal condition of Q_1 at input voltages lower than 260V rms. Accordingly, at these voltage levels, the circuit works as a standard full-bridge rectifier under capacitive load C_3.

At an input voltage of 260V rms or greater, Point C becomes higher than 2.5V, and IC_1 turns on, diverting and sinking the current from D_2. The gate-to-source voltage of Q_1 drops to approximately 2V, and Q_1 switches off. Now, no current flows to charge bulk capacitor C_3 even if the D_1 bridge-rectifier diodes are forward-biased. The rectified input-ac voltage is higher than the voltage across C_3, but Q_1 is off, the loop is interrupted, and no current flows. Accordingly, the output-dc voltage across C_3 gets limited because no charging current is available.

When the rectified ac-input voltage starts decreasing, it eventually hits the 2.5V threshold level of Point C, and Q_1 again switches on. But current does not flow because the rectifier bridge's diodes are now reverse-biased; the rectified input-ac voltage is less than the voltage across C_3. The voltage across C_3 decreases at a rate that the output-power level determines. Eventually, the voltage across C_3 and the rectified input-ac voltage intersect at a level when the rectifier bridge's diodes get forward-biased. Q_1 is still on; therefore, charging current starts flowing. A short interval follows, during which both Q_1 and D_1 conduct. The short

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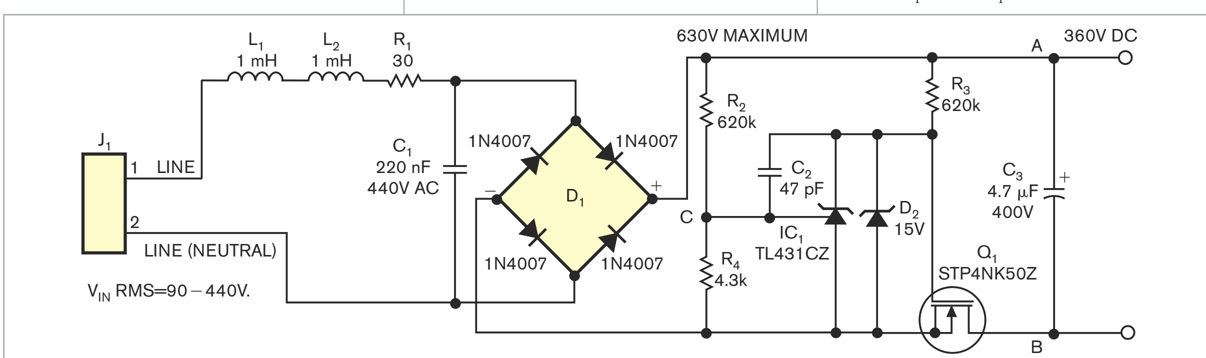

Figure 1 This simple circuit clamps input-ac voltages higher than 260V rms to levels safe for the operation of the power MOSFET in a switched-mode power supply.

charging pulses replenish the energy loss, increasing the voltage to the limited level. When the input voltage gets higher than 260V rms, Q_1 again switches off, and the whole process repeats.

Q_1 has small power dissipation. During every switching period, the MOSFET is on for only 450 μsec, resulting in high efficiency for this high-voltage-limiting circuit. You can use it as a MOSFET switch with the STMicroelectronics (www.st.com) SuperMesh MOSFET STP4NK50Z, which comes in a TO-220 package, but you can also use a Dpak to save space because the MOSFET is not a dissipative-voltage limiter. The current through Q_1 gets interrupted when the 50/60-Hz rectifying diodes are forward-biased. This current interruption causes ringing on the drain-to-source voltage. The clamping circuit passed the conducted EMI (electromagnetic-interference) tests, according to EN 55022 Class B, using peak and average detection. The 1-mH, 0.2A chokes, L_1 and L_2, suppress EMI. The 220-nF, 440V-ac capacitor, C_1, is a simple snubber element across the rectifying diodes of the D_1 bridge. EDN

Autozeroed amplifier with halved noise needs few components

Marián Štofka, Slovak University of Technology, Bratislava, Slovakia

The Analog Devices (www.analog.com) AD8553 autozeroed instrumentation amplifier has a unique architecture in that its two gain-setting resistors have no common junction (**Reference 1**). The first stage of the IC is a precise voltage-to-current converter, in which the first gain-setting resistor, R_1, sets the magnitude of the transconductance. The end stage of the IC is a precise current-to-voltage converter, in which the value of its feedback resistor, R_2, co-determines the overall voltage gain as $G=2(R_2/R_1)$. You can exploit the fact that the two gain-setting resistors are separate and that the input stage is a voltage-controlled current source to lower the component count in amplifiers with extreme noise-reduction demands.

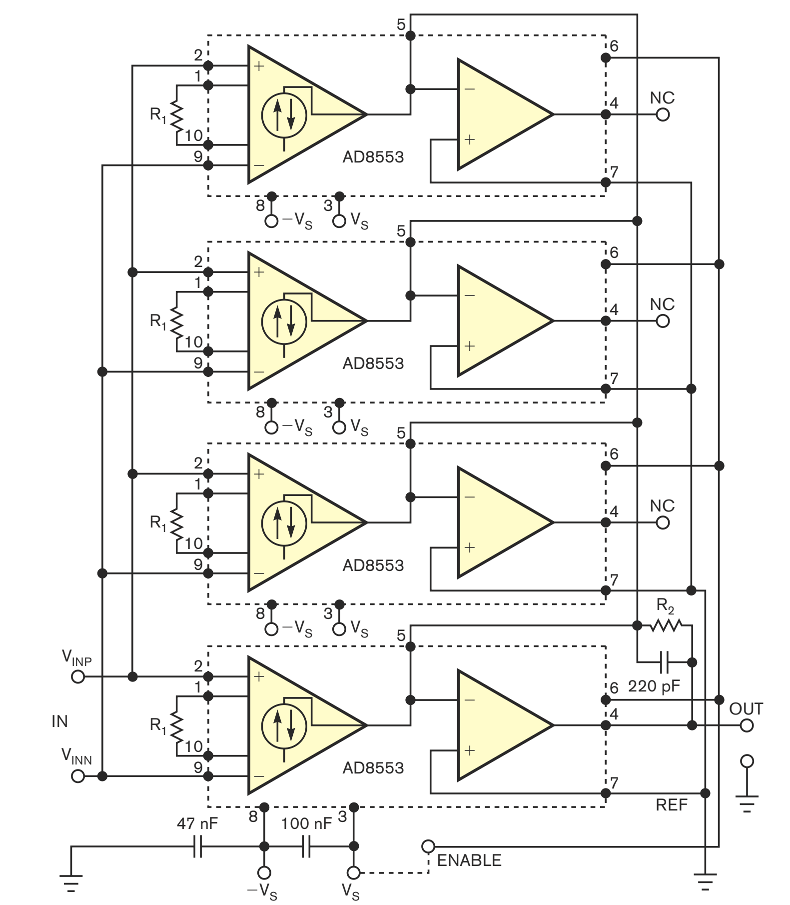

Figure 1 The unique architecture of the AD8553 instrumentation amplifier, incorporating an input-voltage-to-current converter, allows 50% noise reduction with fewer components.

You can use more amplifiers to reduce noise in two ways. First, assume that the sources of random noise in the amplifiers are mutually independent. Further, assume that the noise obeys a gaussian distribution. When averaging the outputs of classic voltage amplifiers, you can reduce the noise to a fraction of $1/\sqrt{N}$ by using N amplifiers and three times as many resistors (**Reference 2**). The internal structure of the AD8553 allows you to use just N+1 resistors for an almost-unlimited number of ICs operating in parallel. By paralleling the respective input pins of more ICs, the connected internal voltage-to-current sources easily operate in parallel (**Figure 1**). The microvolt-range input-voltage-offset mismatch at paralleled input pins of several ICs is harmless here because the output resistances of the voltage-to-current converters are theoretically infinite.

The net result of paralleling N input stages is that they output current of $N(V_{INP}-V_{INN})/(2R_1)$, or N times that of a single IC. You use only one of the current-to-voltage stages of the N ICs. That stage's feedback resistor has the

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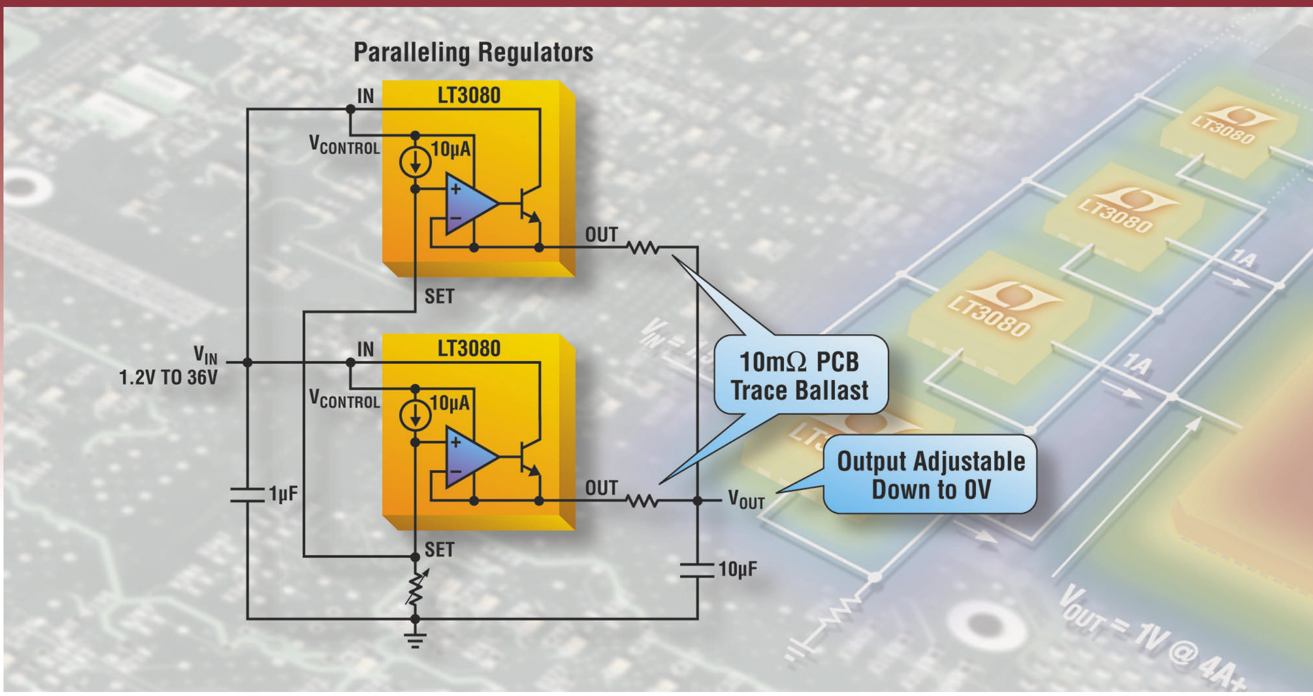

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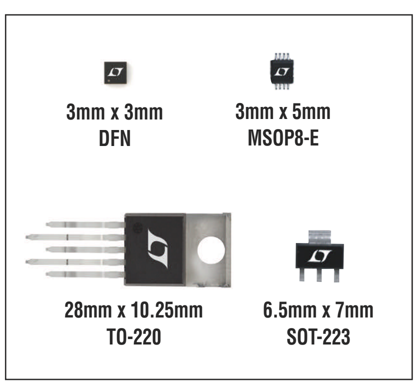

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value of R_2/N, where R_2 is the value for a desired voltage gain of A_V in a single IC. Because the primary source of noise in an amplifying IC is its input stage, you can assume that the standard deviation of the random component of output current of the paralleled-N voltage-to-current converters is $\sigma_{NI}=\sigma_I\times\sqrt{N}$, where σ_I is the standard deviation of the random component of output current of a voltage-to-current converter. These results differ from those in **Reference 2**, in which the authors perform noise reduction by averaging multiple voltages. On the other hand, the deterministic part of current at the common output of the voltage-to-current converters in **Figure 1** has the value of N times that of the single IC. The following **equation** calculates the RSNR (relative signal-to-noise ratio), which you define as the output current over the standard deviation of output noise: $RSNR_N=(N\times I)/(\sigma_I\times\sqrt{N})=\sqrt{N}\times RSNR_I$. It means that, in effect, the noise of the circuit has decreased to a fraction of $1/\sqrt{N}$ compared with that of a single IC. **EDN**

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Buck regulator controls white LED with optical feedback

Dhananjay V Gadre, Netaji Subhas Institute of Technology, New Delhi, India

There is much interest in LED-based lighting due to the availability of high-power, high-efficiency white—and other-color—LEDs (**Reference 1**). Because an LED is a current-controlled device, typical control circuits regulate the current through the LED to maintain uniform intensity. To optimize available power, users often operate the LEDs with a switching-converter circuit—either a buck or a boost converter—depending on the input-dc voltage. **Figure 1** illustrates the configuration of typical buck- and boost-converter white-LED-driver circuits. Adding the resistance, R, in series with the white LED sets the current through the LED. The value of the resistance depends on the desired LED current and the feedback voltage that the buck/boost converter requires. For example, the required resistance is 12Ω for a 100-mA average current through the LED and a 1.23V feedback voltage.

To reduce the power dissipated in the series resistance, engineers often employ the circuit configurations in **Figure 2**. In this configuration, the amplifier's gain reduces the power dissipated in the series resistor by a factor equal to the gain (**Reference 2**).

The circuit configurations in **figures 1** and **2** work well in regulating

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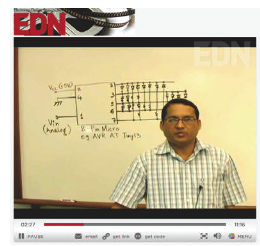

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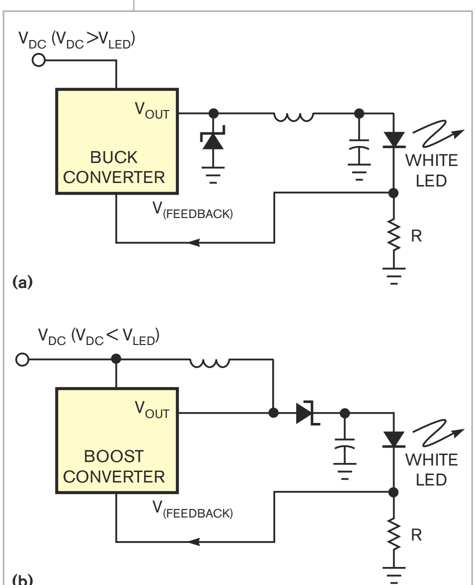

Figure 1 Depending on the input voltage, buck (a) or boost (b) regulators drive high-intensity white LEDs.

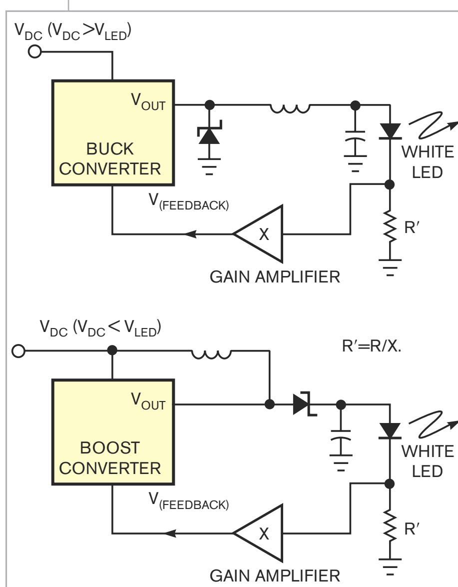

Figure 2 In these circuits, an amplifier gain reduces the power dissipated in the series resistor by a factor equal to the gain.

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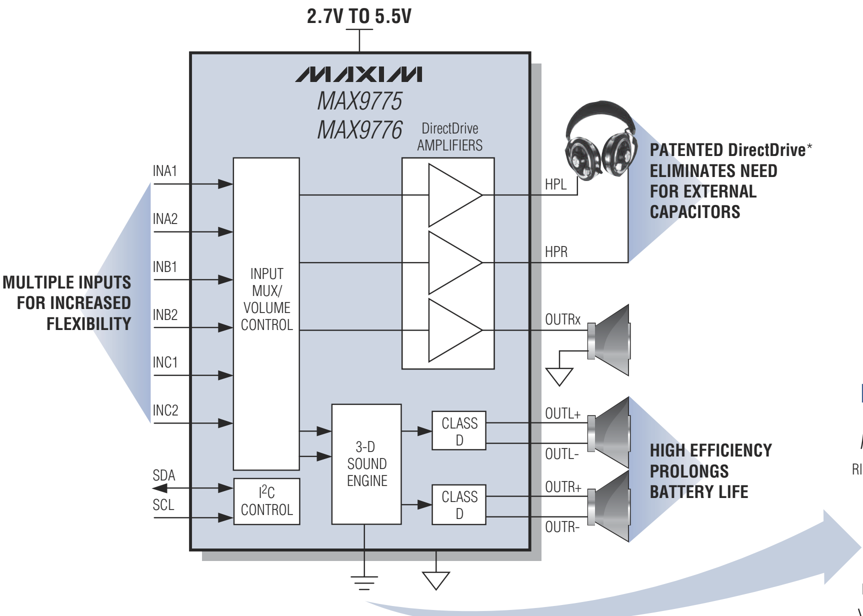

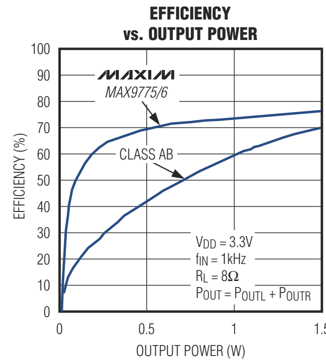

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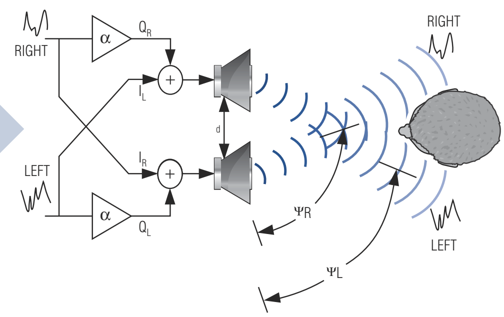

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the current through the LED, provided that the ambient temperature remains constant. However, white and other-color LEDs exhibit significant variation in luminosity as a function of temperature (**references 2** and **3**). Typical figures for variation in luminosity range from 40 to 150% for a 100°C change in temperature. Thus, if you expect the ambient temperature to vary, regulating only the current through the LED is an inefficient way to control the LED. An alternative is to use optical feedback to control the LED (**Reference 3**).

However, rather than use an expensive light sensor and amplifier circuit, you can use a suitable LED as a light sensor (**Reference 4**). **Figure 3** illustrates a controller for a white LED using an inexpensive buck-regulator IC, an adjustable LM2575. A 3-mm red LED in a transparent package senses the light from a 10-mm white LED. The white-LED spectrum is wide enough to excite the red LED as a sensor. For a test current of 60 mA through the white LED, the red-LED-sensor voltage is approximately 40 mV. Because the circuit uses the red-sensor LED's voltage as a feedback to the buck regulator, you must use an amplifier with a gain of approximately 30 because the internal reference voltage of the LM2575 buck regulator is 1.23V. Resistors R_1, R_2, and R_3 control the gain of the amplifier, which comprises an inexpensive LM358 dual op amp. The input-dc voltage powers the op amp. Resistors R_1, R_2, and R_3 have values of 270, 560, and 10 kΩ, respectively. Because R_2 is a variable resistor, changing its setting changes the gain and, thus, the current through the white LED. Thus, R_2 acts as brightness control. The amplifier gain ranges from 28 to 84, depending on the setting of R_2.

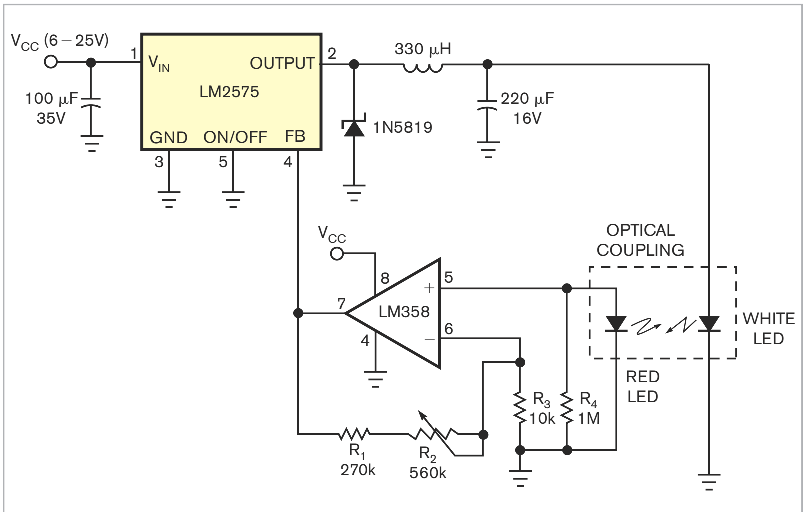

Figure 3 Use an inexpensive buck regulator and a red LED as a sensor for optical feedback to control the intensity of a white LED.

The red LED as a sensor mounts on the side of the white LED itself, thereby using only a fraction of the emitted light from the white LED. File the 3-mm red LED's top to get a flat surface, and then use a drop of superglue to secure the 3-mm red LED onto the side of the white LED.

The LM2575 buck regulator works by changing its duty cycle to regulate the output voltage. If the white-LED output light falls because of increased temperature, the red-LED sensor's voltage falls proportionately. The output of the red-LED sensor connects to the feedback input (Pin 4) of the regulator IC, and, in response, the regulator IC increases the duty cycle of the output voltage you apply to the white LED, thus stabilizing the light. In case of a decrease in ambient temperature, the white-LED light increases, and the regulator reduces the output voltage, which stabilizes the white-LED light.EDN

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2 "Specifications for Nichia Warm White LED," Nichia Corp, www.nichia.com/specification/led_lamp/NSPL510S-E.pdf.

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Routines directly measure microcontroller-bus clock

Kerry Erendson, Bulova Technologies

The Freescale HC08 and newer HCS08 microcontroller families have versatile peripheral modules. Their clock generators are no exceptions. They range from the internal clock, which frees I/O pins, to external crystals or oscillators. Once you select the timing source, you have many options for controlling the final bus frequency. For instance, connecting a 32,768-Hz crystal to an MC9S08GB microcontroller allows you to use the FLL (frequency-locked loop) to generate many bus frequencies as high as 18.874 MHz.

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DS28E01-100**	1kb EEPROM with SHA-1	1-Wire	Bidirectional SHA-1 challenge and response
DS2401/DS2411	64-bit ROM serial number	1-Wire	Customized 64-bit ROM
DS28CM00	64-bit ROM serial number	I²C/SMBus	Customized 64-bit ROM
DS2431	1kb EEPROM	1-Wire	Customized 64-bit ROM, WP/OTP modes
DS2460**	SHA-1 coprocessor	I²C	Secure storage of system secrets

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Selecting the source, the divisors, and the FLL settings allows versatility but also can get complicated.

Once you write the bus-clock-initialization routine, you may want to verify that the bus is running at the speed you intend before moving on to the rest of the project. This Design Idea presents routines that output a square wave at exactly one-tenth the bus speed on any I/O port (**listings 1** and **2**). Just connect a frequency counter to this pin, and it will display your bus frequency. All you have to do is move the decimal point one place to the right. Once you verify the bus speed, you can confidently write the timer, serial-I/O, and other clock-dependent routines.

You need to write code only to first disable interrupts and disable the COP (common on-chip processor). In your bus-clock-initialization routine, be sure to initialize the I/O port you want to use as an output. Then, just jump to the toggle clock, which outputs the bus frequency divided by 10 until power-down. This Design Idea uses PB0 in the HC08 version and PD0 in the HCS08 version. You can use any available I/O port by altering the first line to identify the port and the second line to choose a bit. Also, this Design Idea names ports with the older notation PB, instead of today's more fashionable PTB.EDN

LISTING 1 CODE FOR HC08

```
;TOGCLK - toggle PB0 at 1/10th the bus clock freq. (square wave)
;(NEVER ENDS)

TOGCLK   LDHX #PB        ;put 16-bit address of PB in H:X
         LDA #$01        ;make whatever bits in PB that will toggle=1
TOG01    CLR ,X          ;2
         NOP             ;1
         NOP             ;1
         NOP             ;1
         STA ,X          ;2
         BRA TOG01       ;3
```

LISTING 2 CODE FOR HCS08

```
;TOGCLK - toggle PD0 at 1/10th the bus clock freq. (square wave)
;(NEVER ENDS)

TOGCLK   LDHX #PD        ;put 16-bit address of port PD in H:X
         LDA #$01        ;make whatever bits in PD that will toggle=1
TOG01    STA ,X          ;2
         NOP             ;1
         CLR ,X          ;4
         BRA TOG01       ;3
```


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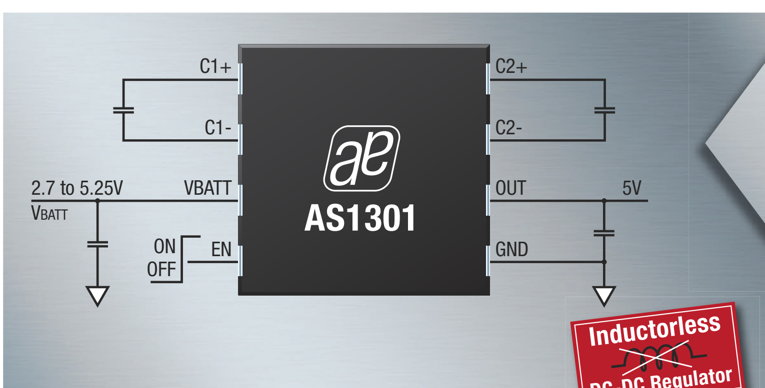

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AS1301-BWLT	92	50	2.7 to 5.25	5	✓	WL-CSP-8

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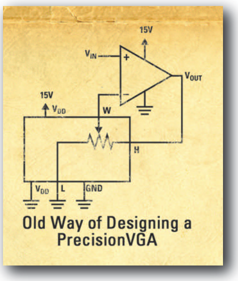

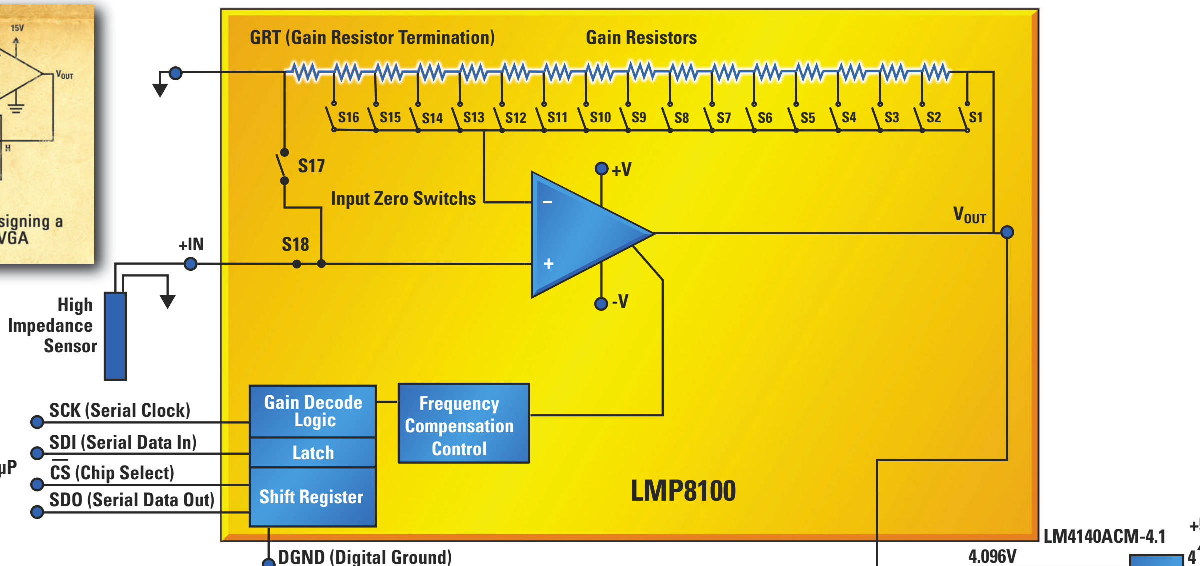

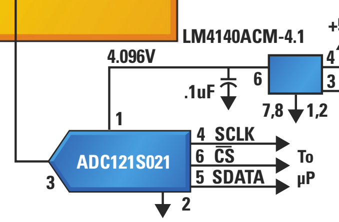

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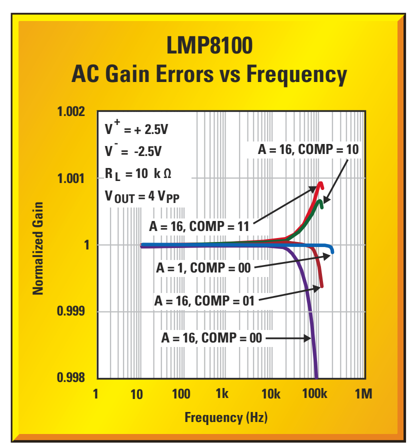

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DESIGN NOTES

Pushbutton On/Off Controller with Failsafe Voltage Monitoring

Design Note 427

Victor Fleury

Introduction

Have you had the exasperating experience of a laptop or PDA defiantly not responding to your commands? You frantically press key after key, but to no avail. As hope turns to anger (but just before you throw the company's laptop through the window) you slam your finger against the on/off power button. Ten seconds later, your laptop finally surrenders and the screen goes black in a high pitched whimper.

The unresponsive pushbutton was likely the result of an unresponsive µP or system logic—as evidenced by the crash. By pressing and holding the on/off pushbutton, the LTC2953 provides the user with the ability to force system power off, even under fault conditions. This long pushbutton command works independently of system logic and automatically shuts off power after the adjustable timer expires. The length of time the pushbutton must be held low in order to force a power down is adjustable with an external capacitor on the PDT pin.

Pushbutton Challenges

The ON/OFF pushbutton of electronic devices presents the system designer with a unique set of challenges. The circuits that monitor the pushbutton translate the chattering pushbutton signal into a clean voltage step that enables a DC/DC converter or turns on a power switch. These circuits communicate with system logic to make sure that power turns on and turns off in an orderly manner. Additionally, failsafe features should disable system power if there is a problem with either the input or output power supply. The pushbutton monitor must also be rugged: absorb high levels of electrostatic discharge, tolerate voltage transients below ground and operate at high voltage levels.

The LTC2953 pushbutton on/off controller with voltage monitoring addresses all of these issues by providing a complete solution for interfacing to the on/off pushbutton of electronic devices. This tiny IC integrates the timing circuitry needed to clean up the pushbutton chatter and provides a simple communication protocol for orderly system power turn on and turn off. The LTC2953 includes a deglitched lockout comparator that prevents the system from drawing power from a dead battery or low supply. The device also provides a single adjustable supply reset monitor with 200ms delay.

The LTC2953's wide input voltage range (2.7V to 27V) is designed to operate from single-cell to multicell battery stacks, thus eliminating the need for a high voltage

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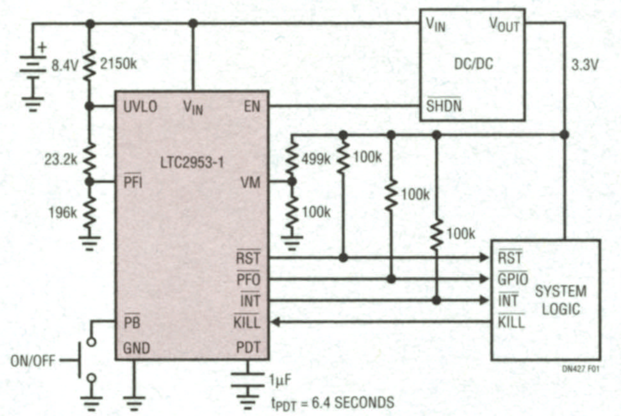

Figure 1. Typical Application

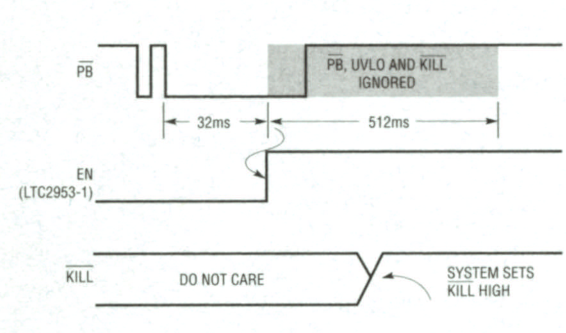

Figure 2. Orderly Power On

LDO. The part's feature set allows the system designer to turn off power to all circuits except the LTC2953, whose low quiescent current (14µA typical) extends battery life. The device is available in a space saving 12-lead 3mm × 3mm DFN package.

Orderly Power On

The rugged pushbutton input of the LTC2953 connects directly to the electronic device's noisy, chattering mechanical on/off switch. To turn on system power, the LTC2953 asserts the enable output 32ms after detecting the end of pushbutton chatter. Once power has been enabled, the system must set the KILL input high within 512ms. This 512ms timeout period is a failsafe feature that prevents the user from turning on the electronic device when there is a faulty DC/DC converter or an unresponsive microprocessor. The LTC2953 turns off power if KILL is not set high during this time window. See Figure 1's application circuit and Figure 2's timing diagram.

Orderly Power Off: Short Interrupt Pulse

Under normal conditions, an electronic device is turned off by pulsing the on/off power switch. To turn off system power, the LTC2953 asserts the interrupt output 32ms after detecting the end of pushbutton chatter. Upon noticing this interrupt signal, system logic performs power down and housekeeping tasks and asserts KILL low when done. The LTC2953 subsequently releases the enable output, thus turning off system power (see Figure 3's timing diagram).

Failsafe Features

The LTC2953 provides 3 comparators for voltage monitoring: UVLO, Power Fail and Reset. The UVLO comparator detects 3 types of aberrant behavior at the input supply. If the supply glitches for longer than 32ms, the LTC2953 will issue an interrupt signal. If the supply falls and stays below the user adjustable level, the LTC2953 will turn off system power after the user-adjustable timer expires. Additionally, the UVLO comparator prevents a user from turning on system power if the input supply is too low (see Figure 4). The power fail is a general purpose uncommitted comparator, useful for distinguishing between a PB interrupt and a low supply interrupt. The reset comparator is a single adjustable voltage monitor with fixed 200ms delay.

Conclusion

The LTC2953 is a low power, wide input voltage range (2.7V to 27V) pushbutton on/off controller with input and output voltage monitoring. The LTC2953 provides a simple and complete solution for manually toggling power of many types of systems. Desirable features include a power fail comparator that issues an early warning of a decaying supply, along with a UVLO comparator that prevents a user from turning on a system with a low supply or dead battery. The LTC2953 provides even greater system reliability by integrating an adjustable single supply supervisor. Two versions of the part accommodate either positive or negative enable polarities. The device is available in a space saving 3mm × 3mm DFN package.

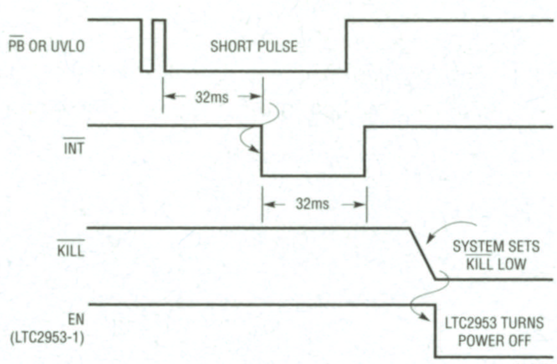

Figure 3. Orderly Power Off

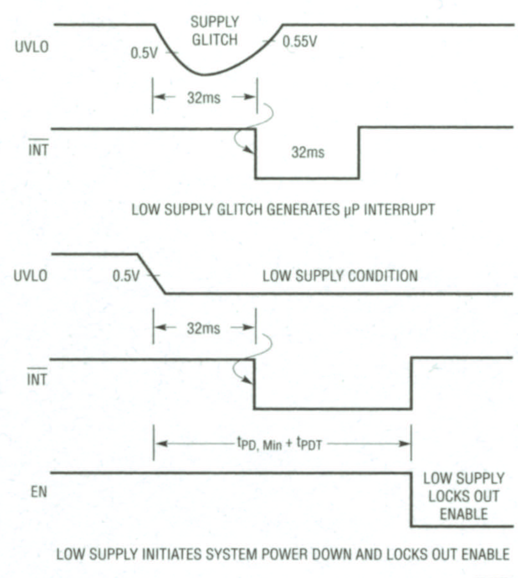

Figure 4. Multifunction UVLO Comparator

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OPTOELECTRONICS/DISPLAYS

Triple-output LED driver targets RGB lighting and LCD backlighting in portable devices

Driving tricolor RGB LEDs for enhanced LCD backlighting, the NCP5623 triple-output LED driver has an I²C interface and built-in gradual dimming. The device suits portable-system applications, including cell phones and MP3 players. With a ±0.5% typical matching tolerance and 32 current levels, the unit's three independently controlled outputs allow 32,000 colors with a tricolor RGB LED. The device includes an integrated gradual-dimming function that progressively increases or decreases output current, producing a theatrical fade-in/fade-out effect. The driver has 94% peak efficiency with less-than-1-μA standby current over a lithium-based-battery operating range. Available in a 2×2×0.55-mm LLGA-12 package, the NCP5623 costs 55 cents (3000).

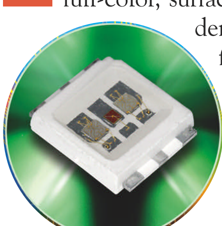
On Semiconductor, www.onsemi.com

830-nm laser diodes use passive NAMs to prevent COMD

Based on the vendor's QWI (quantum-well-intermixing) technology, the HPD6020 high-power, single-emitter laser diode provides 830±5-nm wavelengths and 200 mW of output power. The QWI technology increases the quantum-well bandgap of a semiconductor laser in a controlled manner, allowing the creation of active and passive sections in the same laser cavity. The device creates passive NAMs (nonabsorbing mirrors) at the facet regions of the cavities to avoid COMD (catastrophic optical-mirror damage). The HPD6020 costs $200.

Intense Ltd, www.intenseco.com

Full-color LED package provides independent control for high outputs



Providing a 130° viewing angle, the OVSPRGBCR4 full-color, surface-mount LED package allows independent control of each color for high output from each chip. It also allows for programming the color mix to achieve all the colors of the rainbow plus white. Comprising red, green, and blue LEDs, the RGB LED package has water-clear lenses mounted on top. The device features 21-, 32-, and 7.5-lm luminous flux

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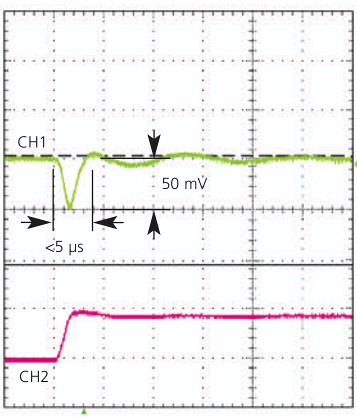
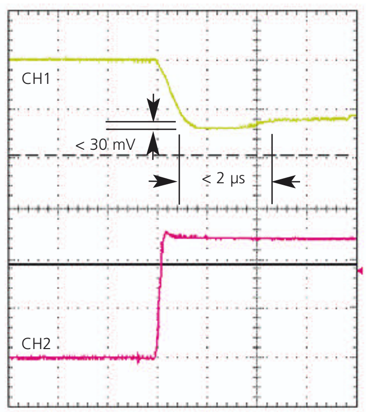


CH1: V_{OUT} 50 mV/div Timebase: 5 µs
CH2: I_{OUT} 50 A/div

48 V_{IN}, 1.2 V_{OUT}, 0-40 A at 10 A/µs
Less than 50 mV undershoot and recovery in <5 µs using 330 µF ceramic C_{OUT}.

Load Line Recovery



CH1: V_{OUT} 100 mV/div Timebase: 1 µs
CH2: I_{OUT} 40 A/div

48 V_{IN}, 1.2 V_{OUT}, 0-100 A at 600 A/µs
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V048F015T100	1.5	0.81 - 1.72	100	91.0
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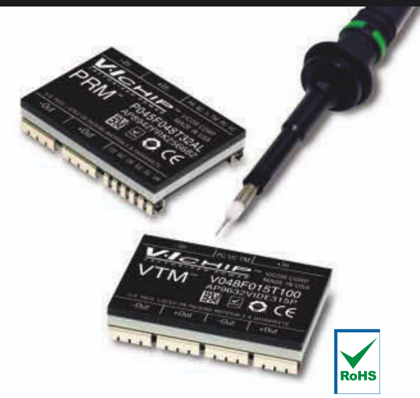

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OPTOELECTRONICS/DISPLAYS

for red, green, and blue LEDs, with a 7-, 11-, and 2.8-cd typical on-axis intensity, respectively. Features include a 250-mA dc forward current per color, a 500-mA peak-pulsed-forward current, and a 20K/W thermal resistance. Supporting a 125°C maximum rated junction temperature, the device has a −40 to +100°C operating-temperature range. Measuring 6×6×1.5 mm, the OVSPRGBCR4 power-LED package costs $4.

Optek Technology, www.optekinc.com

White-LED drivers target medium- and high-brightness systems

Claiming a 91% efficiency at maximum load for improved thermal conditions, the multistring SC440 and SC441 white-LED drivers power display-backlight applications in notebook-computer and LCD panels. The SC440 can power six strings of 30-mA white LEDs in series, making the device suitable for displays as large as 15 in. The SC441 powers four strings of 150-mA white LEDS in series and suits automotive-navigation screens and other screens as large as 9 in. The devices feature a 4.5 to 21V input range, a 2.5A built-in power switch, extensive protection mechanisms, and a PWM (pulse-width-modulation) dimming control with 50-kHz frequencies, allowing a 0.2 to 100% linear brightness. The SC440 and SC441 each cost $2.13 (1000).

Semtech, www.semtech.com

Step-up dc/dc converters have 92% efficiency

Claiming 92% efficiency, the MAX8901A/MAX8901B step-up dc/dc converters drive a string of two or six white LEDs. Enabling 1-μF input capacitors and 0.1-μF output capacitors, the converters drive 1.5- to 4-in. LCDs in battery-operated devices, such as PDAs, GPS (global-positioning-system) devices, smartphones, and digital cameras. Features include a single input enabling the IC and controlling LED intensity and 0.1-μA power consumption in shutdown mode. With the LED current proportional to the PWM (pulse-width-modulation) duty cycle, the MAX8901A uses a direct-PWM input for regulating LED intensity. The MAX8901B uses single-wire, serial-pulse dimming, reducing LED intensity in 32 linear steps; the devices have a 24.75-mA full-scale LED current for serial-pulse dimming at 0.75-mA per step. Available in 2×2-mm TDFN-8 packages, the MAX8901A and MAX8901B converters cost $1.25 (1000) each.

Maxim Integrated Products, www.maxim-ic.com

Charge-pump-based white-LED drivers aim at affordable headsets

Targeting affordable handsets, the AAT3193 is the first in a family of two- and three-channel, charge-pump-based white-LED drivers. Driving three LEDs at 30 mA each, the driver supports the illumination of low-cost, monochrome, and highly opaque TFT (thin-film-transistor)-LCD panels. The driver features 10% part-to-part current accuracy and 3% channel-to-channel current matching. These charge-pump-based devices automatically switch between 1 and 2× mode, improving efficiency and minimizing the number of required external components. Available in a 2×2-mm, 10-lead SC70JW package, the AAT3193 driver costs 49 cents (1000).

Advanced Analogic Technologies, www.analogictech.com

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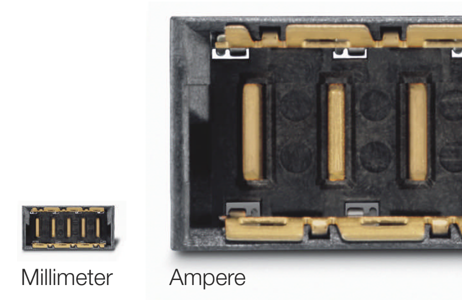

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TEST AND MEASUREMENT

Synchro/resolver-to-digital converter has eight measurement channels

The 74SD3 synchro/resolver-to-digital converter comes on a conduction-cooled PMC. The converter provides eight independent, programmable synchro/resolver tracking-converter-measurement channels. Each channel features 16-bit resolution, ±1-arc-minute accuracy, a 150-rps tracking rate, accurate digital-velocity output, and wrap-around self-test. The 74SD3 costs $3158 (100).

North Atlantic Industries, www.naii.com

Embedded-software-verification platform provides multiple interface features

The Stride 2.1 scalable embedded-software-verification platform enables the development software for wireless digital handsets supporting standard cellular technology and push-to-talk two-way radio service. Features include remote interfacing with access to both function-call APIs and messaging interfaces, on-target-interface tracing with profiling and record-and-playback functions, and a dynamic-interface interception for simulating or replacing embedded-software interfaces. These features allow for exercising the code during implementation without writing test code. The Stride 2.1 platform costs $8300, and current Stride 2.0 licenses are eligible for an upgrade at no cost.

S2 Technologies, www.s2technologies.com

TDC includes six independent stopwatches

Adding to the vendor's Acqiris product line, the TC890 multistart, multistop TDC (time-to-digital converter) features six independent stopwatches that provide timing measurements for start events and multiple-stop events at high resolution. The converter records multiple events, or "hits," per input channel, with 50-psec timing resolution and 15-nsec mean dead time between sequential pulses on the same input at double-pulse resolution. Running at full speed, the device offers a 25 million-event/sec data-throughput rate. The TC890 TDC costs $13,700.

Agilent Technologies, www.agilent.com

EMBEDDED SYSTEMS

MEMS accelerometer suits motion-activated user interfaces

The LIS202DL digital-output two-axis linear accelerometer targets a range of low-g applications in consumer and industrial markets, including motion-activated user interfaces, gaming in portable devices, and vibration monitoring. The MEMS (microelectromechanical-system) accelerometer features click and double-click recognition, motion-detection/wake-up, and highpass filters. Turning on the configurable highpass filters enables motion-activated functions and vibration monitoring, regardless of whether the end product is tilted or upside-down during measurement. A sensor with an embedded motion-detection/wake-up feature reduces power consumption in products that power on or off during or after being touched or moved. Other features include a digital output through standard SPI/I^{2}C, a 10,000g shock survivability, and a choice of ±2 and ±8g acceleration ranges. Available in a 5×3×0.9-mm LGA-14 plastic package, the LIS202DL costs $3 (10,000).

STMicroelectronics, www.st.com

Intersil Video Drivers

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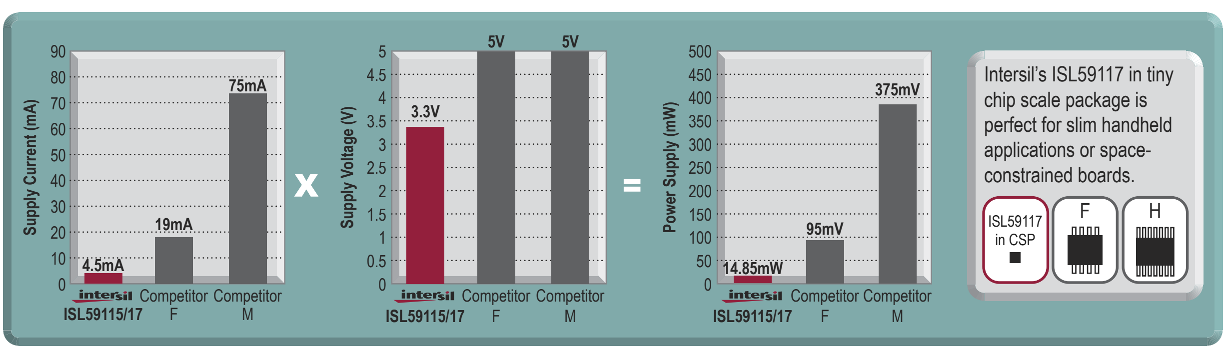

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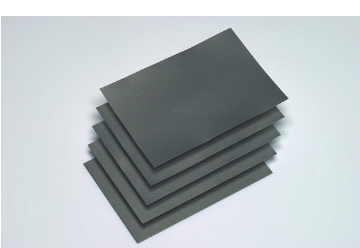

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productroundup

EMBEDDED SYSTEMS

Quadrature-encoder input board provides A, B, and Z inputs per channel

Suiting use with the vendor's PowerDNA, UEILogger, and UEIPCA data-acquisition and -control cubes, the four-channel DNA-Quad-604 quadrature-encoder input board provides standard A, B, and Z index inputs for each channel. Able to handle quadrature applications with a 16.5-MHz maximum input frequency and 32-bit counters, the device includes four digital inputs, in addition to the four A, B, and Z channels, and eight digital outputs. The digital-I/O lines suit use as auxiliary digital inputs and outputs, or you can configure them as trigger-in, trigger-out, or clock-out signals per channel. The digital I/O features 3.3- and 5V-logic compatibility, and the digital outputs supply ±12-mA drive current, 350V isolation, and 7-kV ESD protection. The DNA-Quad-604 costs $695.

United Electronic Industries, www.ueidaq.com

Industrial computer uses AMD Geode LX800 processor

Featuring fanless operation, the Relio R1300 industrial computer uses the high-performance, low-power, 500-MHz AMD Geode LX800 processor. The standard I/O includes two 10/100BaseT Ethernet ports, four USB 2.0 ports, 8-bit GPIO (general-purpose I/O), a parallel printer port, and four serial ports. Using the vendor's SeaI/O modules, local or remote I/O expansion is available in numerous configurations, including optically isolated inputs, Reed and Form C relay outputs, TTL interfaces, analog to digital, and digital to analog. The device communicates with SeaI/O devices using the Modbus RTU (remote-terminal unit), allowing you to place one or more SeaI/O modules with the computer or remotely at altitudes as high as 4000 feet. The Relio R1300 costs $679.

Sealevel Systems, www.sealevel.com

Motion cards deliver high-speed motion trace

The Prodigy motion cards feature advanced trace capabilities, allowing you to store as many as four motion variables at once. They provide real-time, high-speed servo-trace capture with 40 kbytes of onboard dual-port memory. The devices provide board-level one-, two-, three-, or four-axis motion control for dc-brush, brushless-dc, step, and microstepping motors. Available in PCI and PC/104 configurations, the cards costs $380.

Performance Motion Devices, www.pmdcorp.com

INTEGRATED CIRCUITS

System-host board features Intel's Quad-Core processor

Compatible with Intel's Quad-Core processor, the SHB (system-host-board) Express (PICMG 1.3) supports one-, four-, eight-, and 16-lane PCI Express electrical links. A high-bandwidth and -speed design supports a range of PCI Express option cards and bridge chips providing PCI/PCI-X option-card functions. Features include a quad-channel system-memory interface, dual independent 1066/1333-MHz front-side buses, and three 10/100/1000BaseT Ethernet interfaces on LAN ports 1 and 2 of the device's I/O bracket. The SHB costs $5491.

One Stop Systems, www.onestopsystems.com

ELECTRONIC COMPONENTS

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productroundup

INTEGRATED CIRCUITS

Quad PSE controller enables POE applications

Targeting POE (power-over-Ethernet) applications, the MAX5952 quad PSE (power-source-equipment) controller provides 45W of power over standard Ethernet cable. Operating from 32 to 60V, the device provides 802.3af powered-device discovery and classification and supports dc and ac load-disconnect-detection methods. The controller includes Class 4 and Class 5 classification, suiting high-powered devices. Features include an integrated 9-bit ADC with an I^2C-compatible, three-wire serial interface that monitors and reports the current each port draws. A system microcontroller can control the device, or you can configure it for operation in manual or semiautomatic modes. The controller has programmable gate-charge current, current-limit threshold, start-up time-out, overcurrent time-out, and autorestart duty cycle. Providing pin compatibility with the MAX5945, the device also provides undervoltage-lockout protection, overtemperature protection, and output-voltage slew-rate limit during start-up, power-good, and fault status. Available in an SSOP 36, the MAX5952 costs $6.33 (1000).

Maxim Integrated Products, www.maxim-ic.com

Micropower Hall-effect switch has low power consumption

Using CMOS technology allows the MLX90248 Omnipolar Micropower Hall-effect-switch family to deliver a noncontact magnetic switch with microwatt power consumption. Suiting use in flip, slide, and clamshell portable handsets, as well as in PDAs and personal-entertainment devices, the switch detects the opening action, features high magnetic sensitivity, and integrates an on-chip advanced dynamic-offset-cancellation technique. The Omnipolar magnetic sensitivity allows activation using either a north magnetic field or a south magnetic field. The device switches on in the presence of a sufficiently strong magnetic field facing the marked side of the package. The Hall sensor features a 0.5-mT minimum release point and a 6-mT maximum operating point. Additional features include a 2.5 to 3.5V supply voltage, an 8-μA average current consumption at 2.5V, and sensing every 70 msec maximum. Measuring 1.5×2 mm with a 0.43-mm maximum thickness, the QFN package enhances pole-independent performance. Available in a thin SOT-23, a chip-scale-package option, and a QFN package, the MLX90248 costs 31 cents (50,000).

Melexis, www.melexis.com

Capacitance-to-digital converter supports touchpad technology

Targeting cell phones, multimedia players, digital cameras, and other small mobile devices, the AD7147 capacitance-to-digital converter integrates active-shield technology that protects the device from capacitance-to-ground pickup and other noise sources in the systems. The converter features 13 capacitance inputs and femtofarad resolution, supporting scroll wheels, touchpads, sliders, or as many as 36 buttons per device. The AD7147 analog front end provides three times better sensor response than the vendor's previous AD714x products, allowing accurate finger navigation. The converter consumes 1 mA in full-power mode, 50 μA in low-power mode, and 2 μA in shutdown mode. On-chip sensitivity algorithms compensate for changes in temperature and humidity. The AD7147 includes an SPI-compatible serial interface, and the AD7147-1 features an I^2C-compatible serial interface. Available in a 4×4-mm LFCSP-24 package, the AD7147 converter costs $1.30 (1000).

Analog Devices, www.analog.com

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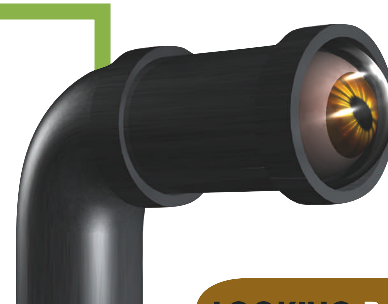
LOOKING AHEAD

TO THE INTERNATIONAL ELECTRON DEVICES MEETING

For more than half a century, the place to find out about the next generation of electronic-circuit elements, from the FET to the latest in quantum-dot technology or alternative nonvolatile memory, has been IEDM (International Electron Devices Meeting, www.his.com/~iedm/). This year's edition, from Dec 10 through 12 in Washington, will headline an in-depth discussion of high-k/metal-gate transistors for 45-nm processes, including Intel's (www.intel.com) first detailed public description of its apparently industry-leading process. TSMC (Taiwan Semiconductor Manufacturing Co, www.tsmc.com) will counter with a description of its 32-nm CMOS-foundry process, which includes the first 2-Mbit SRAM test chip. And STMicroelectronics (www.st.com) will describe a process that allows local use of fully depleted silicon-on-insulator technology within a bulk-CMOS die. In keeping with the growing concern over low power and the environment, a novel session on emerging technologies will feature energy-harvesting devices. The conference is an invaluable window into the near future of electronics.



LOOKING BACK

AT THE CONTINUING SEARCH FOR ALTERNATIVE MEMORY TECHNOLOGIES

A super-high-speed memory device, which responds in a hundred-millionth of a second, utilizes a miniature printed circuit of metallic lead at temperatures close to absolute zero (−459.7F). International Business Machines developed the unit based on the unusual properties of special superconducting materials. Even after developers remove the energy source, current continues to flow in the circuit without diminution. The device requires only one-third the current needed to drive conventional ferrite memory units, while providing an increase in speed of about 100 times.

—*Electrical Design News*, October 1957

LOOKING AROUND

AT HARDWARE'S GROWING ROLE IN SOFTWARE DEBUGGING

Before SOCs (systems on chips), software was not a hardware engineer's problem. Then, along came chips with microprocessors on them, and it was suddenly hardware engineering's responsibility to make sure that code executed on the silicon. Making sure the code was correct to begin with was still somebody else's problem. But now, with the differentiation in end systems increasingly coming from—often hardware-dependent—software, both teams share the responsibility for getting the code right. We are seeing rapid development in hardware features that assist in software debugging, from debugging engines embedded in processor cores to specialized logic analyzers within the SOCs.

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Samsung Memory and Windows Vista… performance worth celebrating

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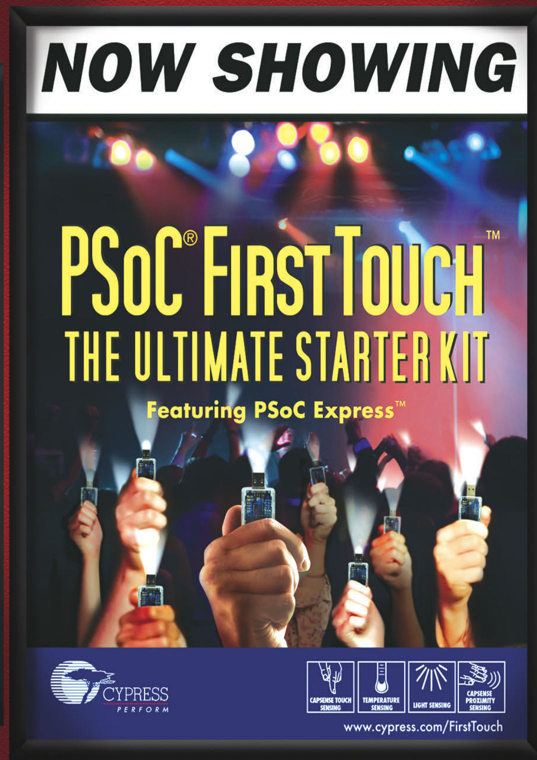

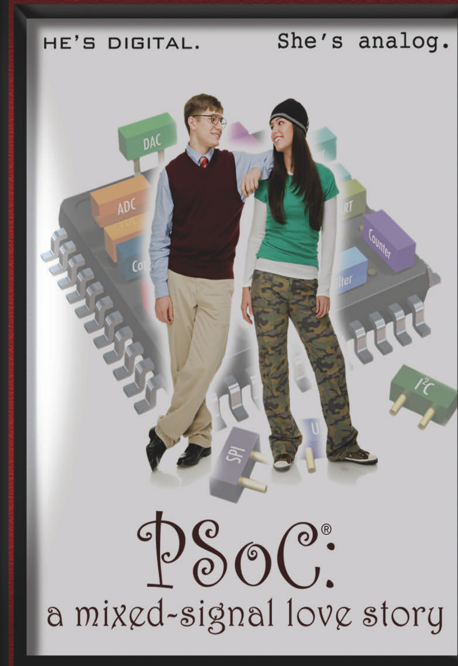

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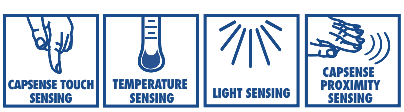

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